

# MS-7B07 Ver:10

**CPU:**  
AMD AM4

**System Chipset:**  
Promontory A320  
(Value DIY or System Builder)

**Main Memory:**  
DDR IV \* 2 MAX:64 GB

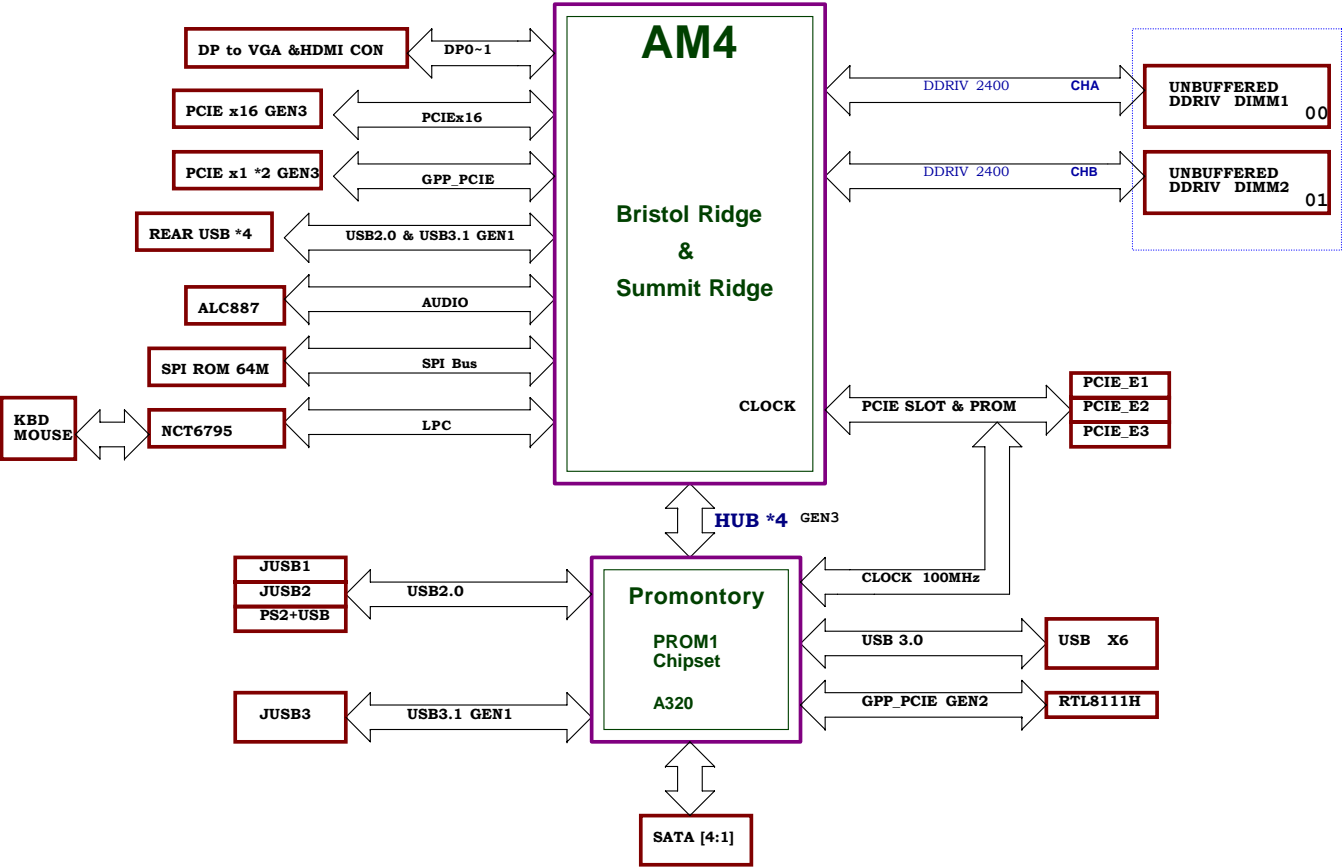
**VRM**  
RT8894 4+2

**On Board Chipset:**  
LPC Super I/O --NCT6795  
LAN RTL8111H  
Azalia CODEC - Realtek ALC887

**Expansion Slots:**  
From CPU  
PCI Express X16 Slot \* 1  
PCI Express X1 Slot \* 1  
PCI Express X1 Slot \* 1

**OCP IC:**  
RT9553B


## FUSION BLOCK DIAGRAM



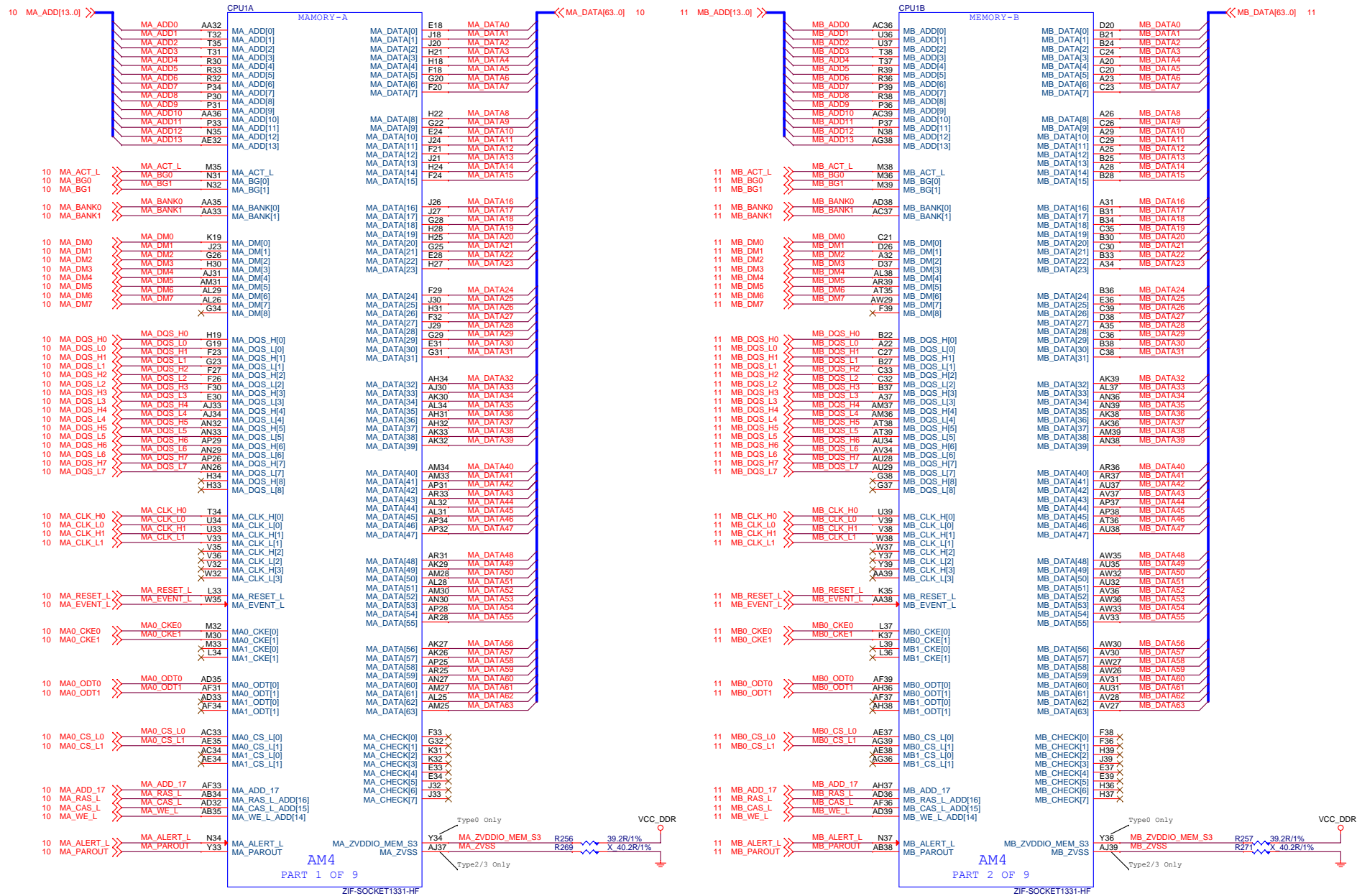


# AMD AM4

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25 USB Rear PS2+USB2.0	
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30 DP to VGA ITE6516	
31 ACPI uPI-5VDIMM&3VSB	
32 PM-NB681-1.05V/GS7133-2.5V	
33 DDR PWR VPP25/VTT-MP2143	
34 DDR Power-RT8231AGQW	
35 CPU Power 1P8V-MP2147	

 <b>MICRO-START INT'L CO.,LTD.</b>		
Title <b>COVER SHEET</b>		
Size	Document Number	Rev
Custom	<b>MS-7B07</b>	<b>1.0</b>
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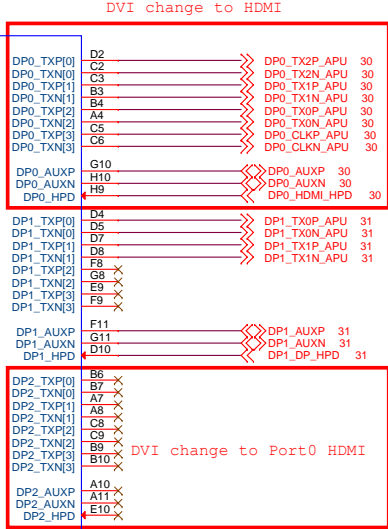
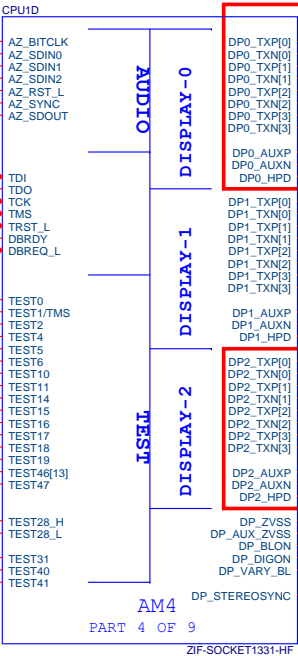
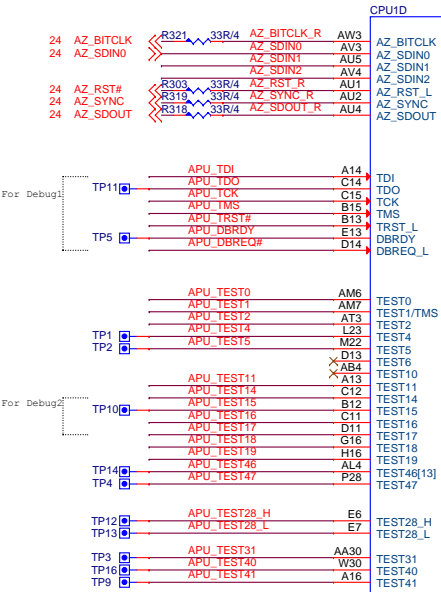
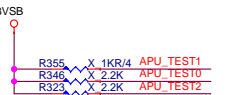
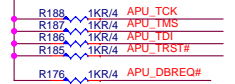
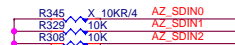


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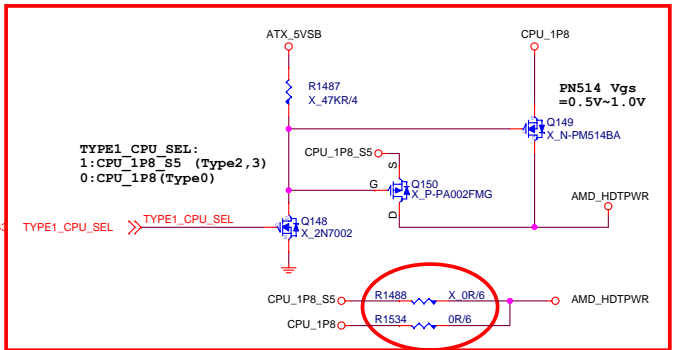


For HDMI

For DP to VGA

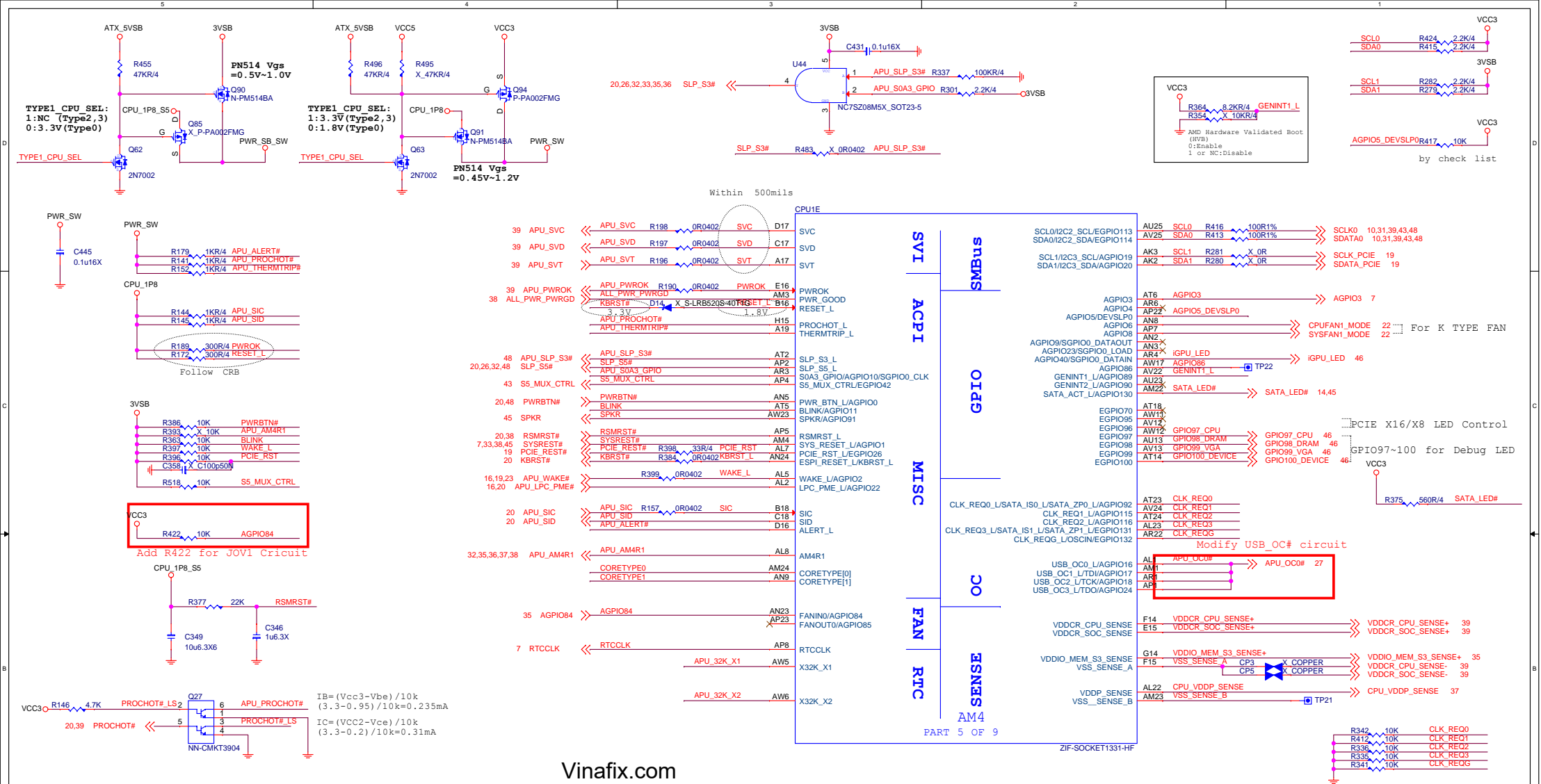
Not supported on AMD Family 17h/Models 00h-0Fh

K14 PIN: T HDMI SPEAKER Pull-up EM



20170414 add R1534





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Layout:Place x'tal within 1.5 inch of APU

## AM4 CPU TYPE Circuit

CPU	TYPE	CORETYPE	0
BR	0	0	0
NA		0	1
SR	2	1	0
RV/ZP	3	1	1

Change by CRB rev. B

CPU\_1P8\_SS

CORETYPE1

TYPE1\_CPU\_SEL

TYPE1\_CPU\_SEL

0:BR/NA

1:ST/RV/ZP

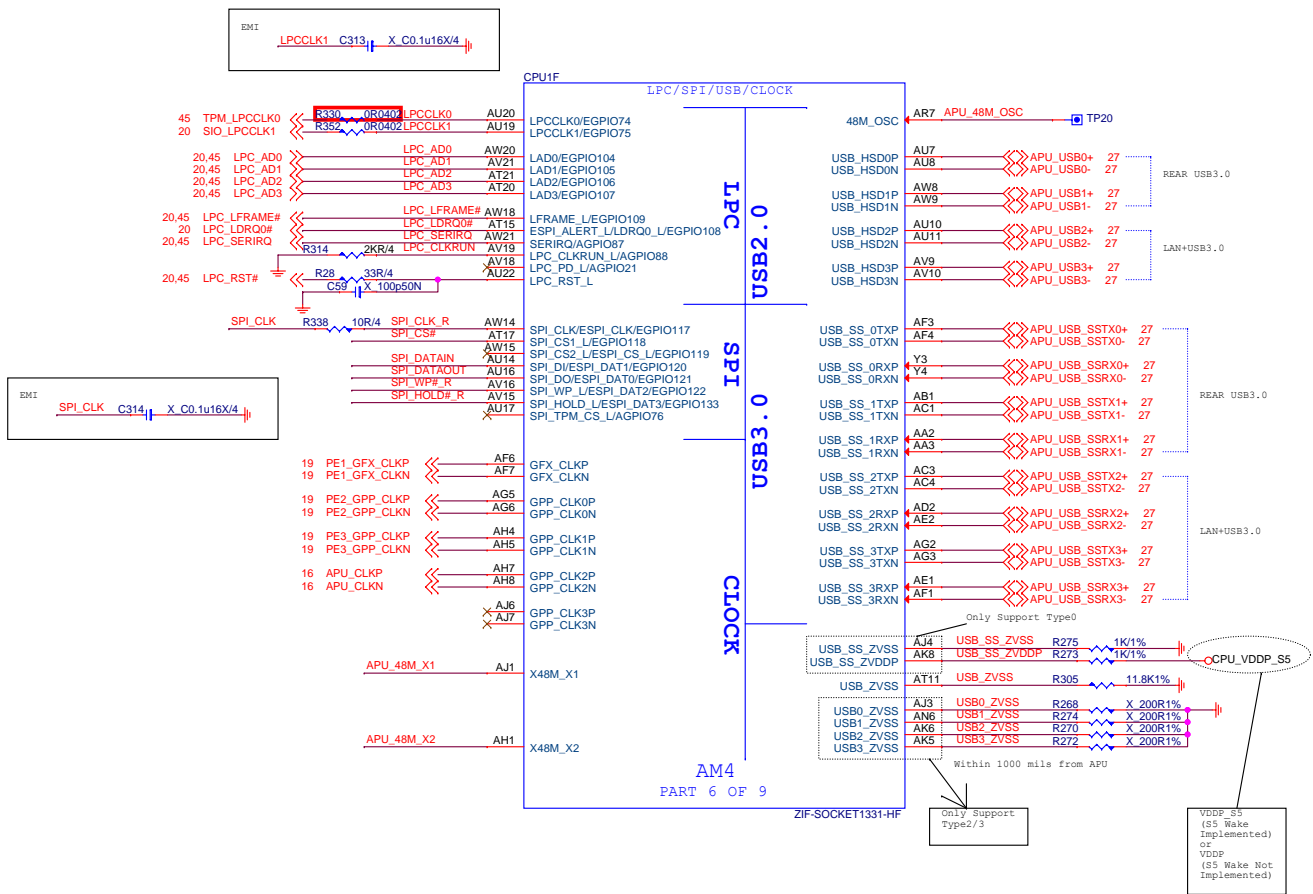
TYPE0\_CPU\_SEL

TYPE0\_CPU\_SEL

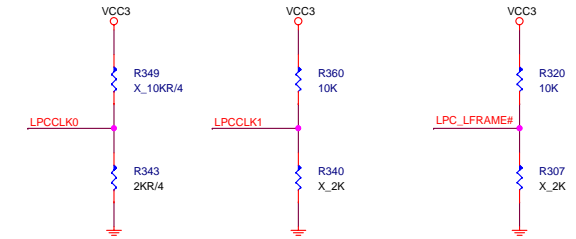
0:BR/SR

1:RV/ZP

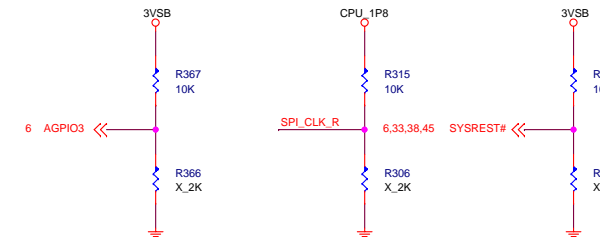




## Strapping Options

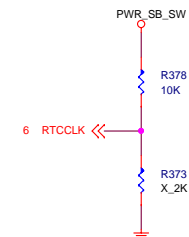
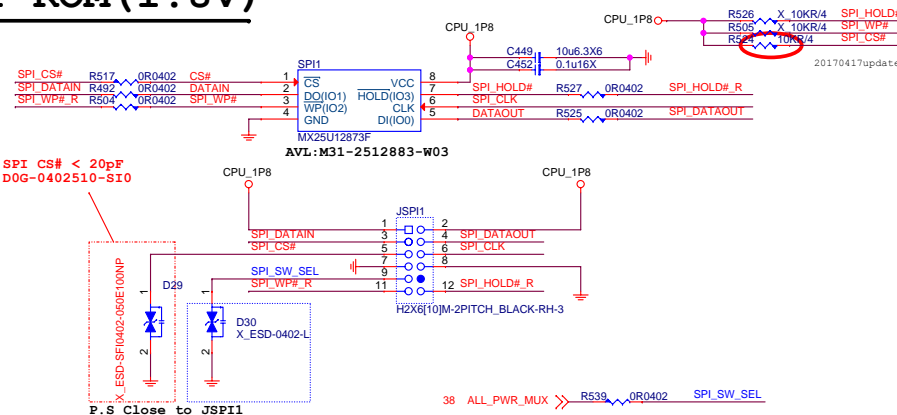


	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator <b>(Default)</b>	SPI ROM <b>(Default)</b>
PULL LOW	LPC device Boot Fail Timer Disabled <b>(Default)</b>	Configured for External clock generator ?????	LPC ROM



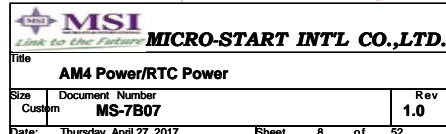
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic <b>(Default)</b>	Use 48Mhz crystal clock and generate both internal and external clocks <b>(Default)</b>	Normal reset mode <b>(Default)</b>
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

## SPI ROM (1.8V)

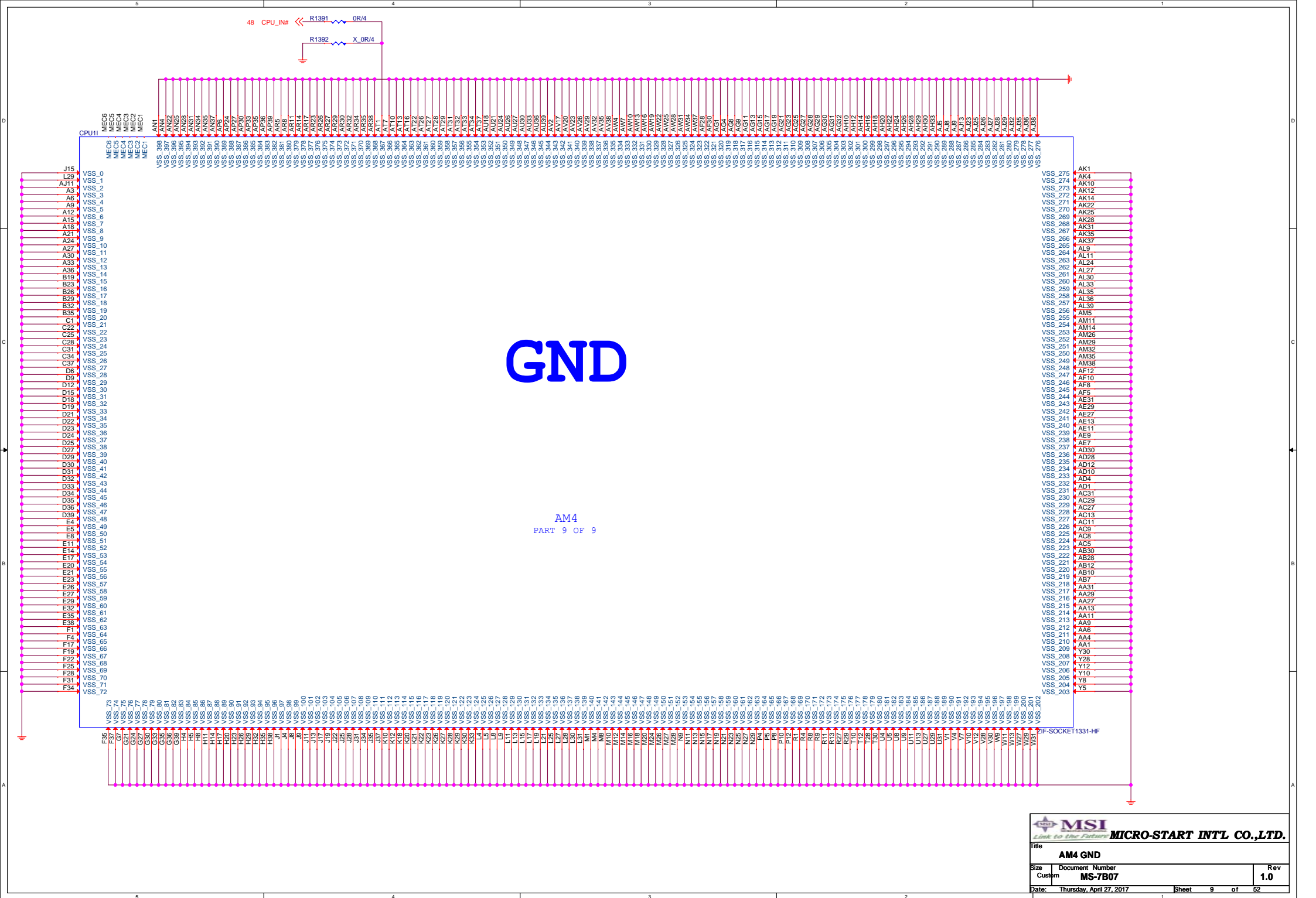


	RTCCLK
PULL HIGH	RTC Coin Battery is on board <b>(Default)</b>
PULL LOW	RTC Coin Battery is not on board



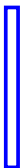




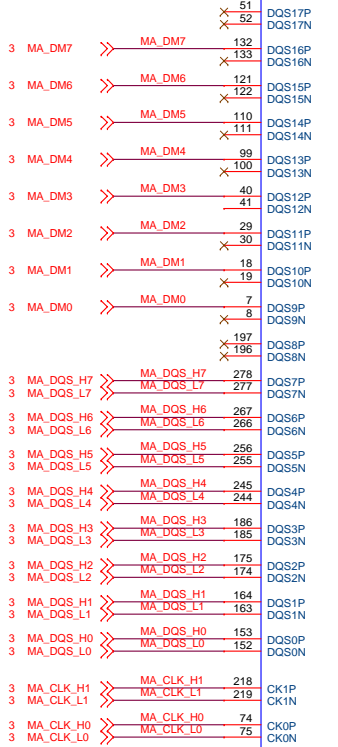




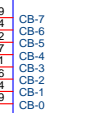
A1



DIMMA1A



C2  
S3\_N\_C1  
S2\_N\_C0



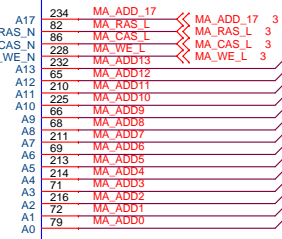
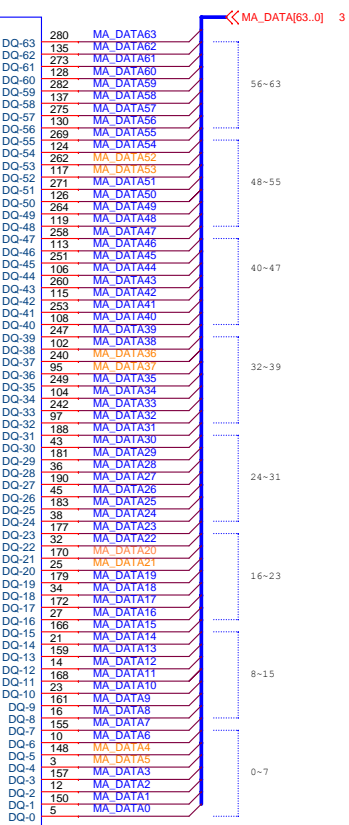
RESET\_N  
EVENT\_N  
ALERT\_N  
ACT\_N  
PAR

SAVE\_N\_NC



DRIV-288P\_BLACK-RH-21

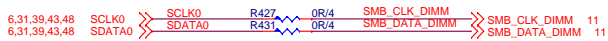
Footprint




SMB\_CLK\_DIMM  
SMB\_DATA\_DIMM



DIMM1 (CHANNEL-A) -A0  
ADDRESS = 0:0 [SA1:SA0]



**MSI**  
*Link to the Future*

**MICRO-START INTL CO.,LTD.**

Title  
**DDR4 DIMM CH-A**

Size  
Custom

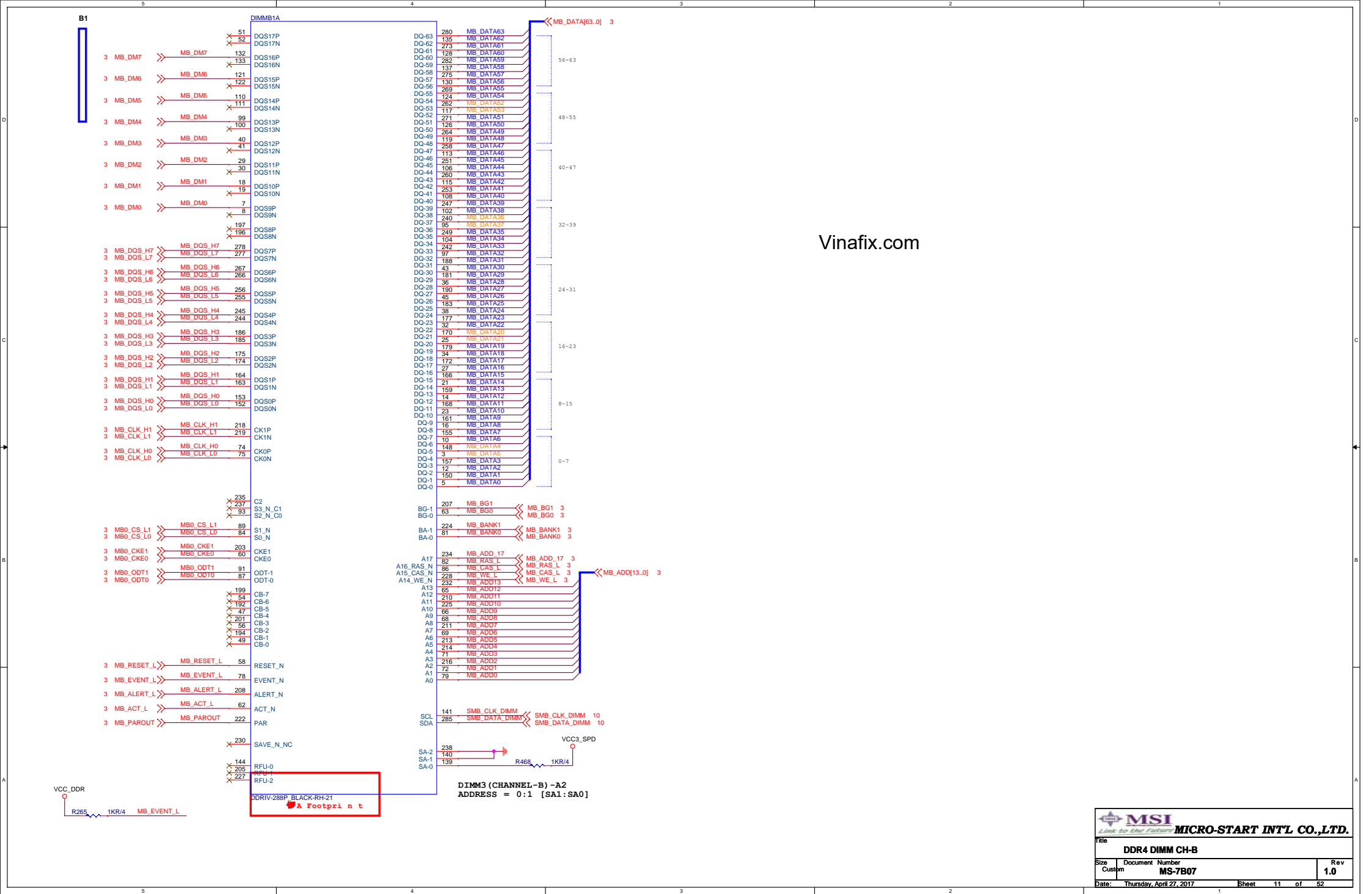
Document Number  
**MS-7B07**

Rev  
**1.0**

Date: Thursday, April 27, 2017

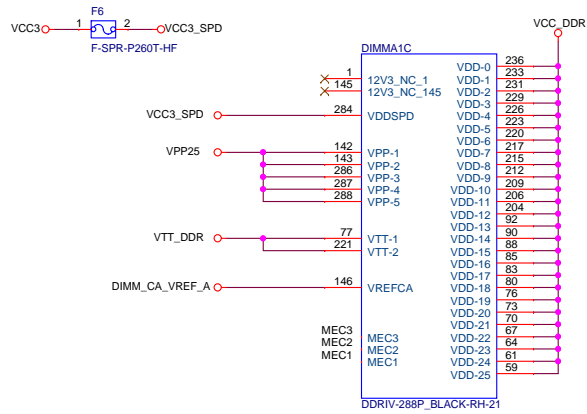
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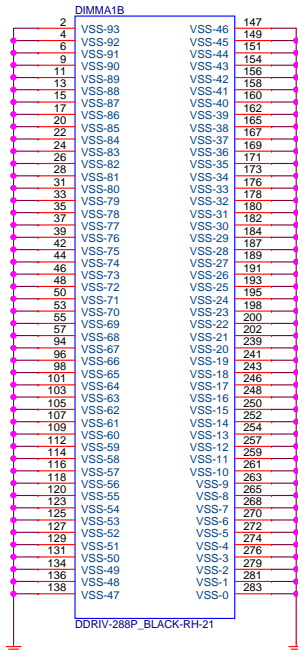
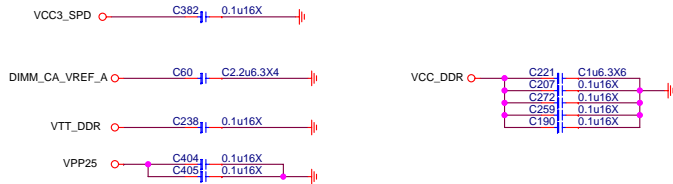


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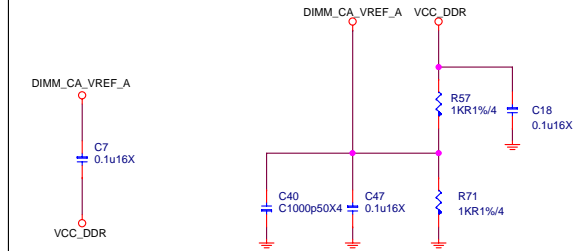


DIMM SLOT PN BY SPEC

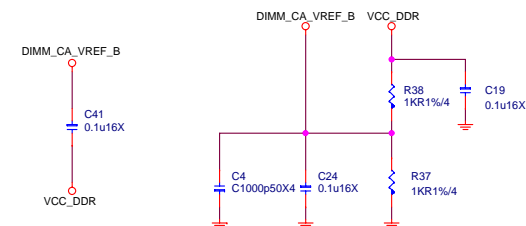
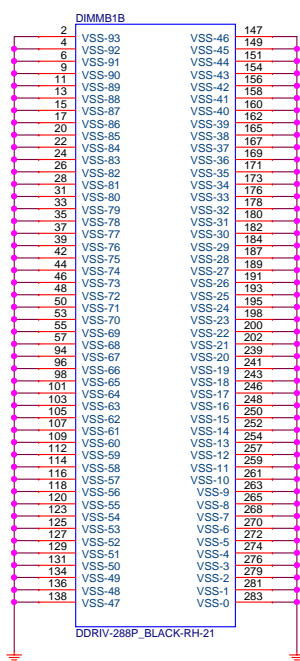


## DDR VREF

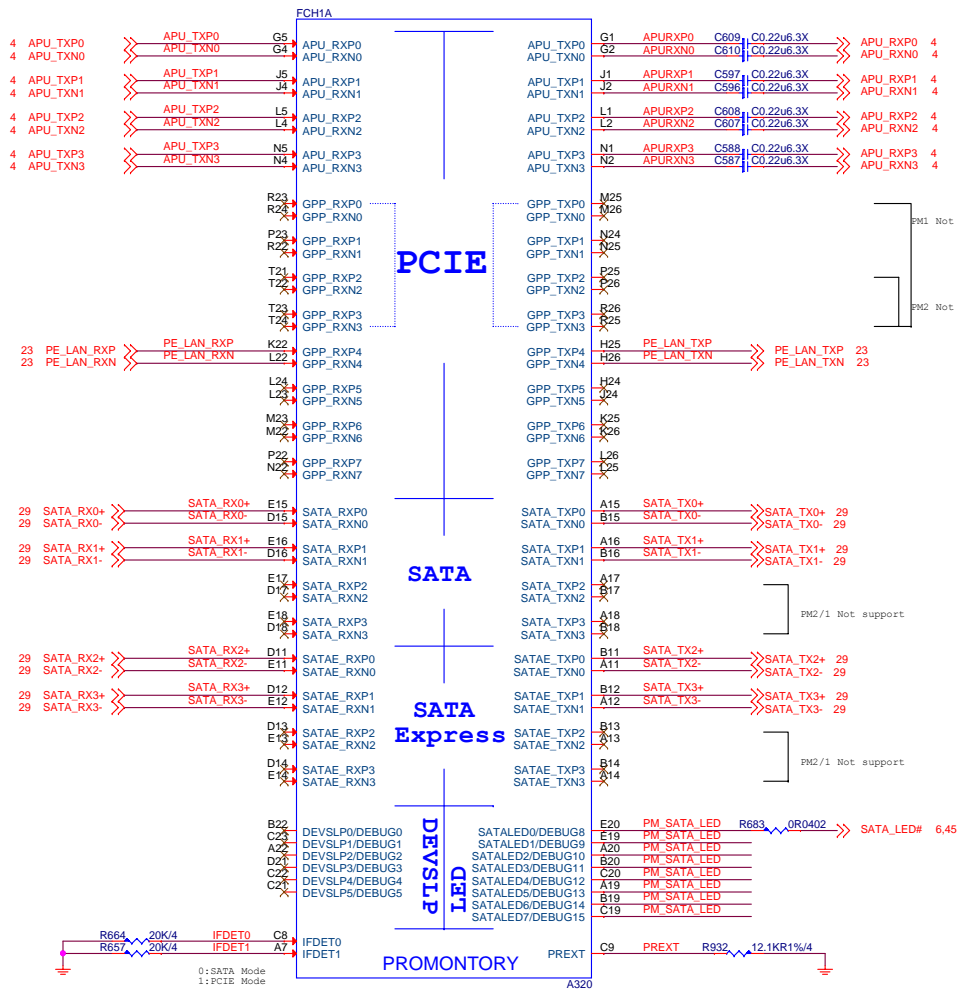
(place resistors close to DIMMs)





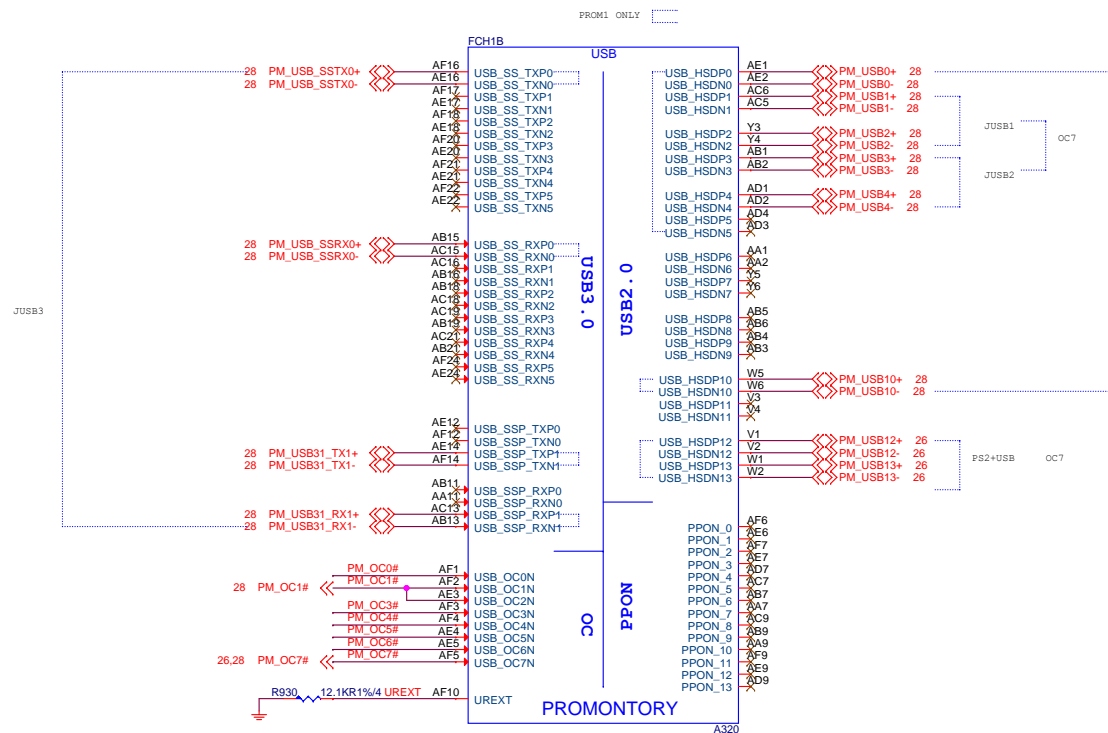
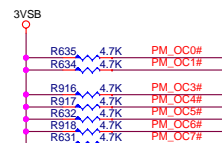




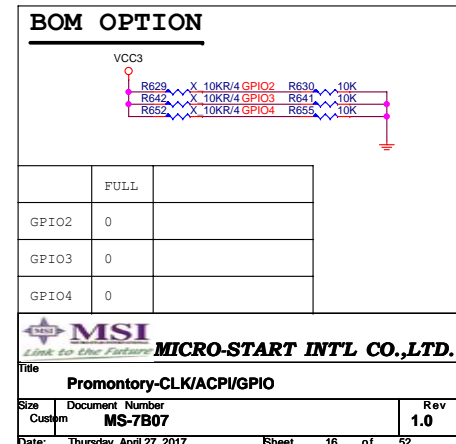
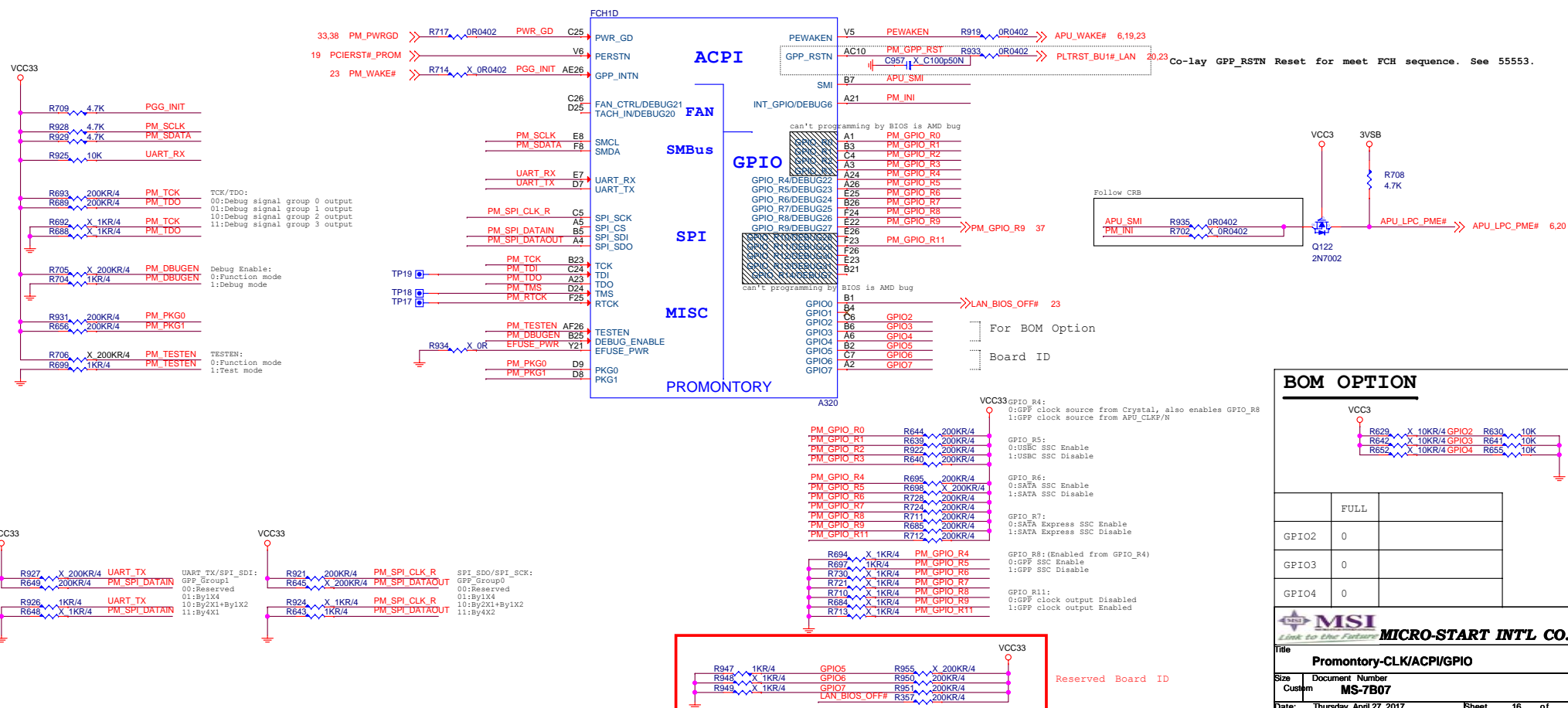
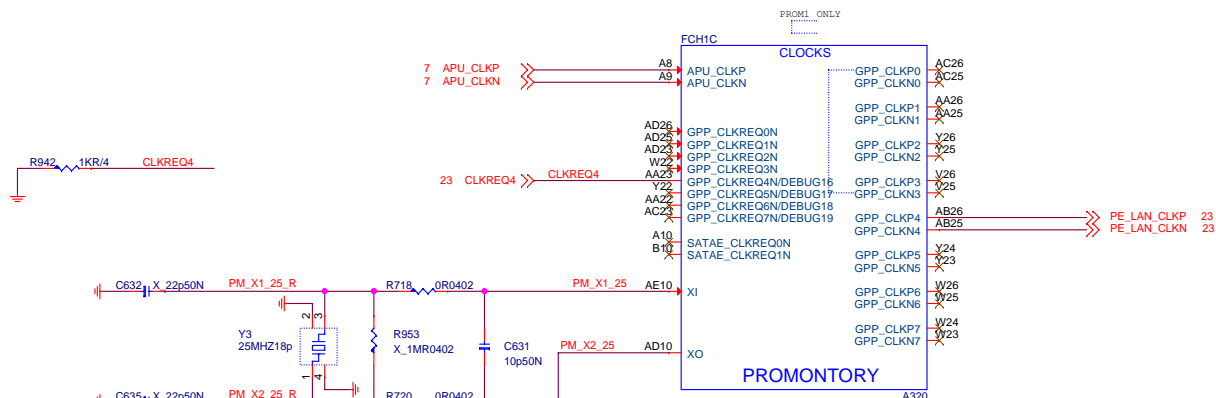


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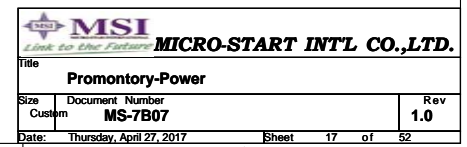














GND

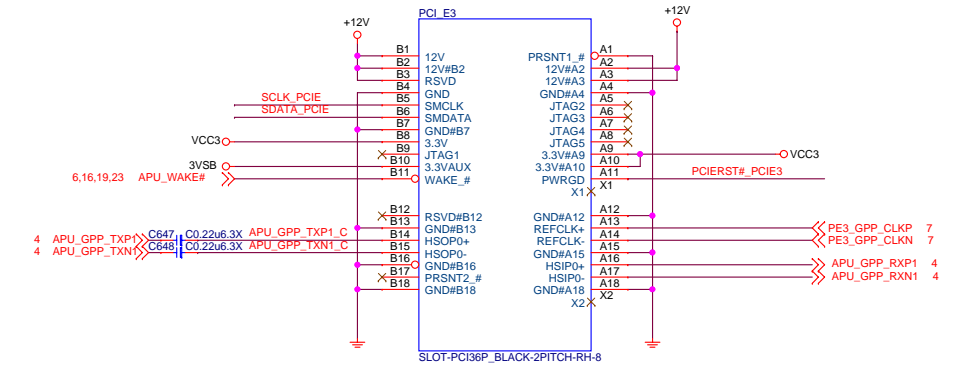
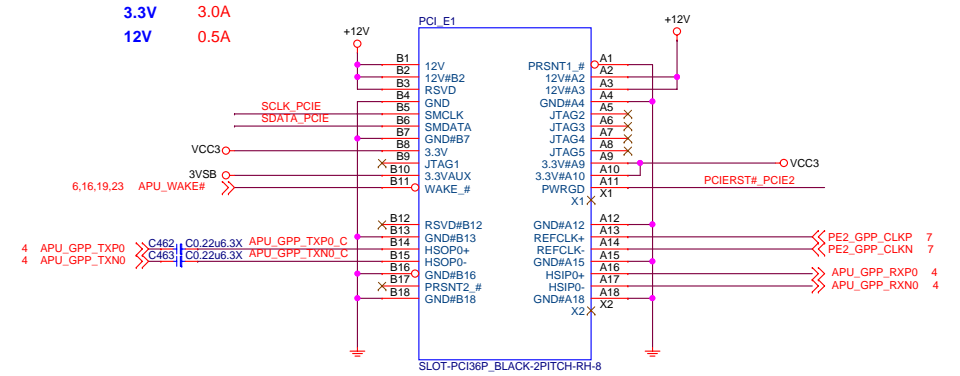
PROMONTORY



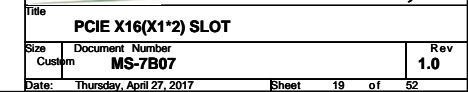
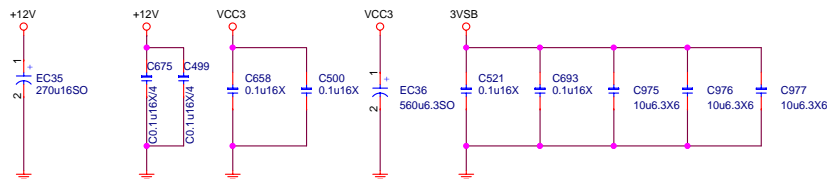
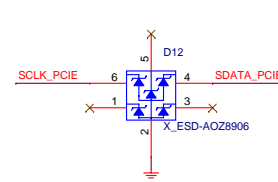
3.3V	3.0A
12V	5.5A

PCIEX1 12V 0.5A  
3.3V weak 375mA

3.3V	3.0A
12V	0.5A

[illegible]

**SMB\_SEL**  
**GPIO Default High**



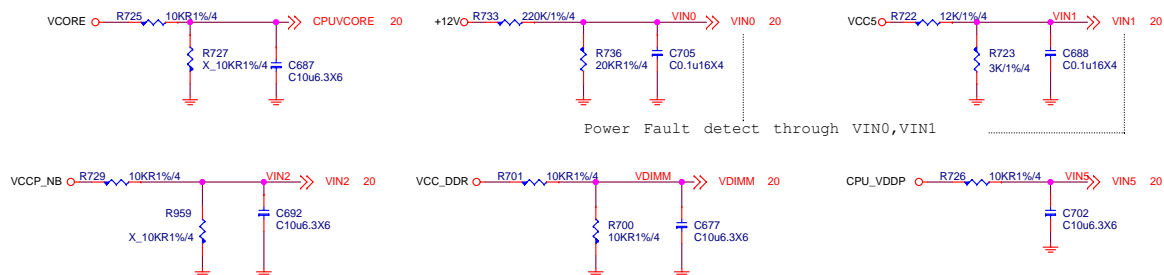






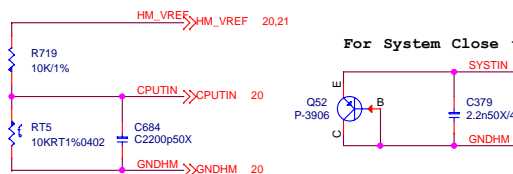
# HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

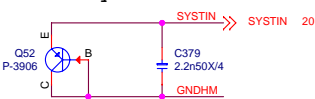


## Thermal Monitor

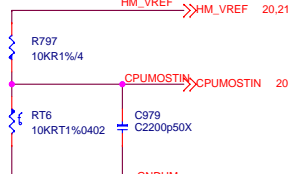
For CPU Under Socket



For System Close to SIO

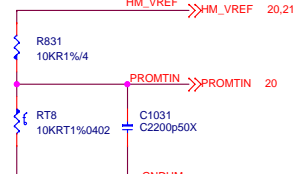


For CPU MOS



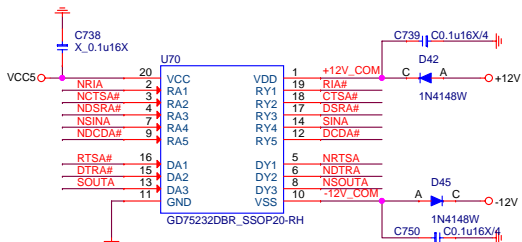
Close to CPU MOS

For PROM

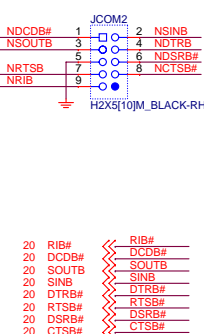
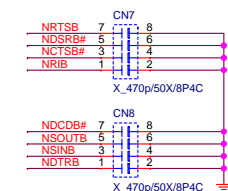
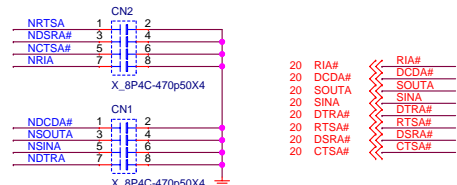
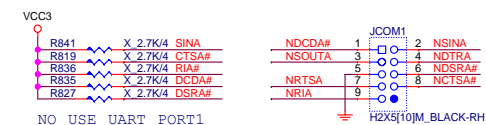
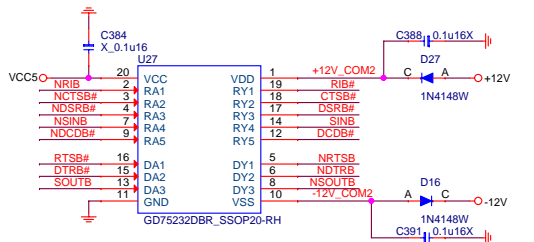


Place to under Promontory

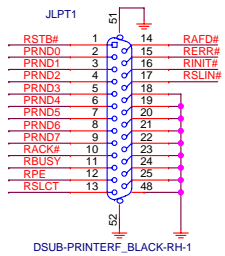
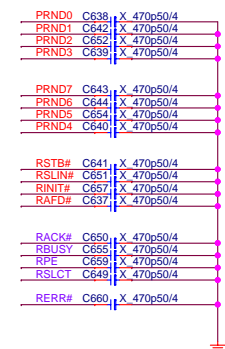
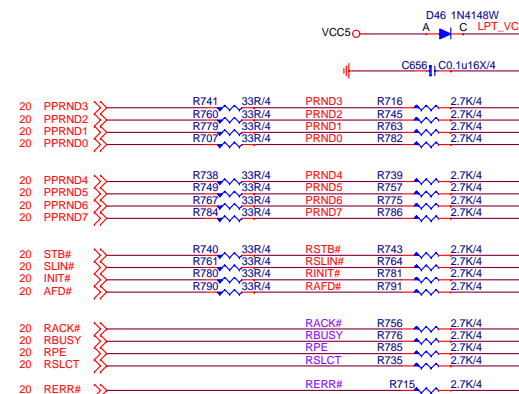
## SERIAL PORT 1



## SERIAL PORT 2

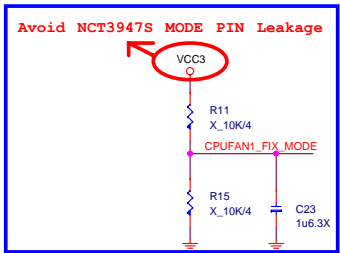


# PARALLAL PORT

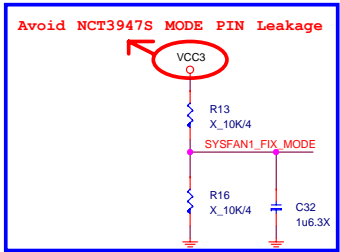




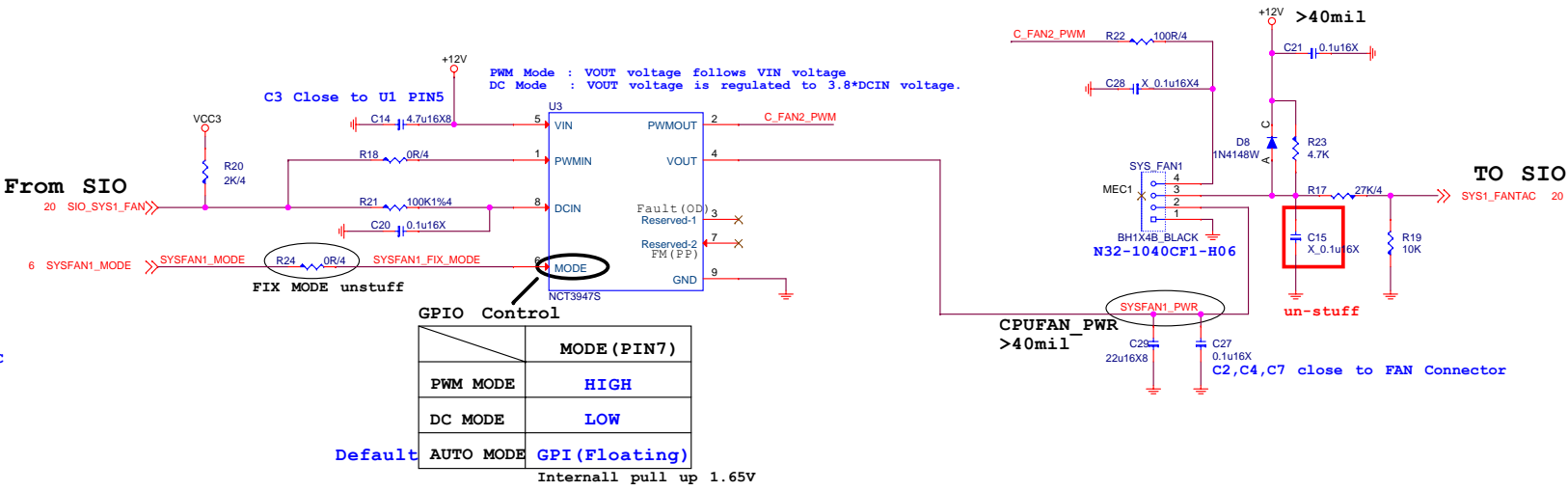
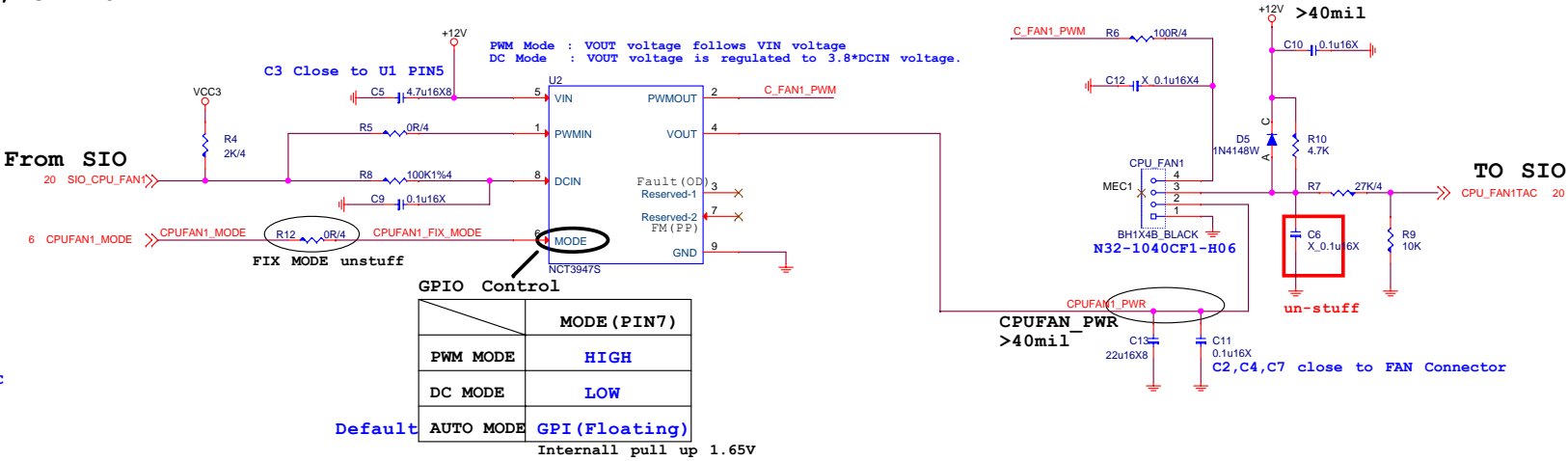
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE  
2.GPIO パワー ち伝 PW M/DC M O D E



Resever For FIX DC or PWM MODE USE By PM SPEC



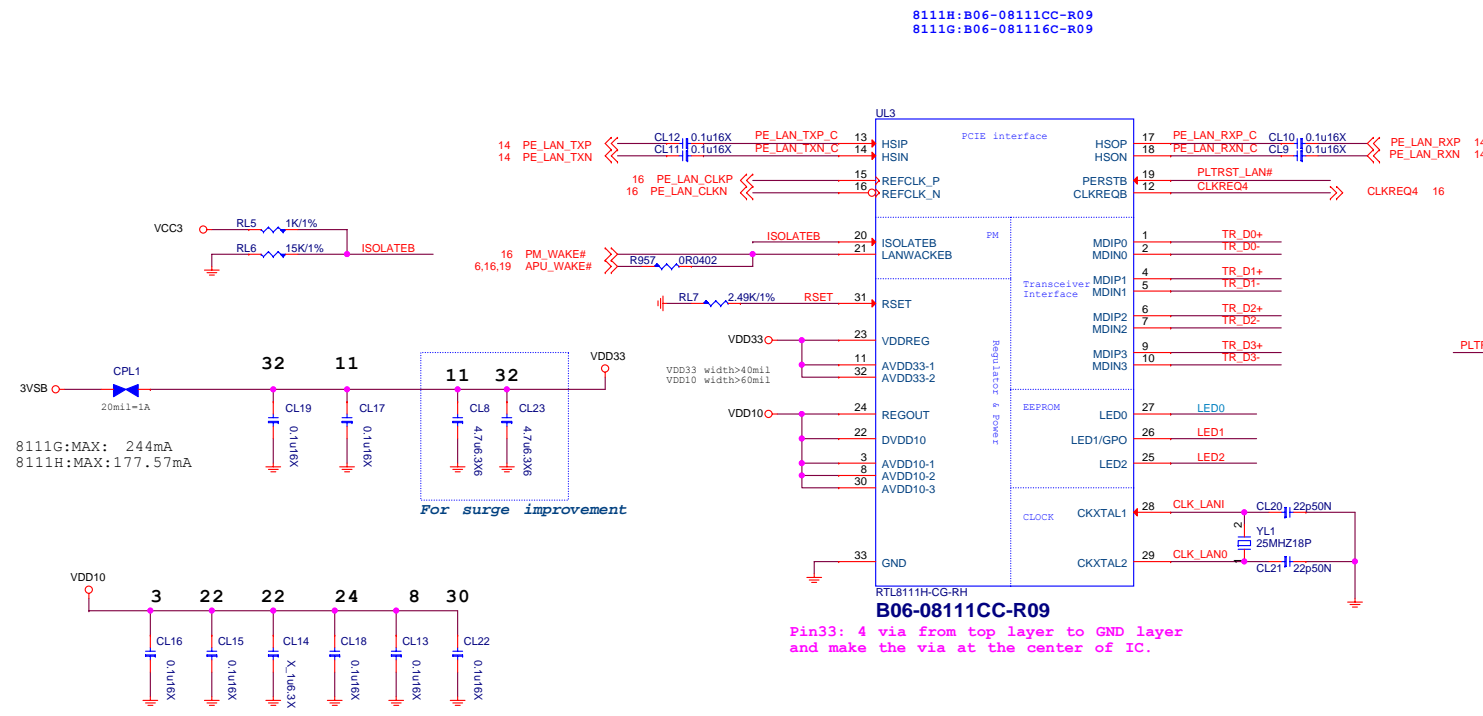
Resever For FIX DC or PWM MODE USE By PM SPEC



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RTL8111G/RTL8111H Giga LAN



8111G:MAX: 244mA  
8111H:MAX:177.57mA

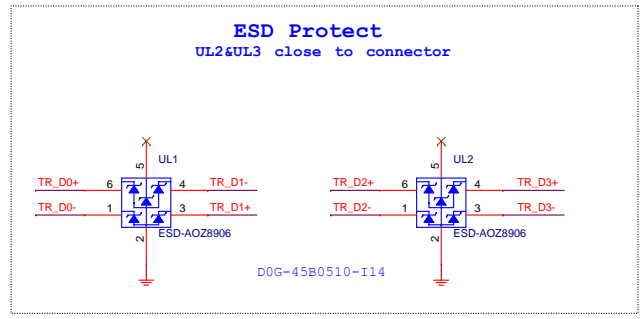
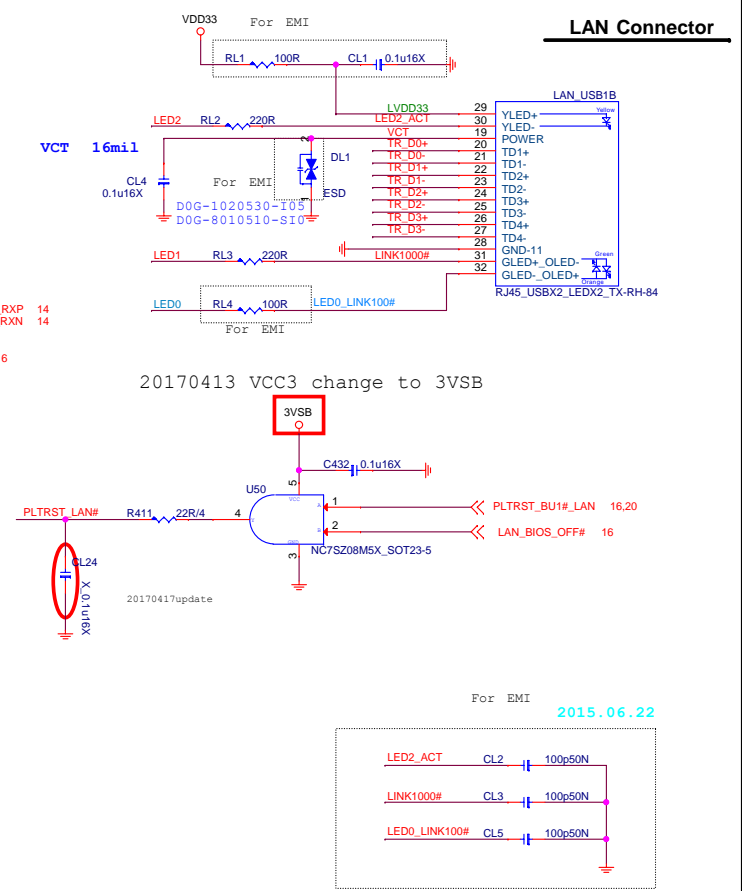
8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

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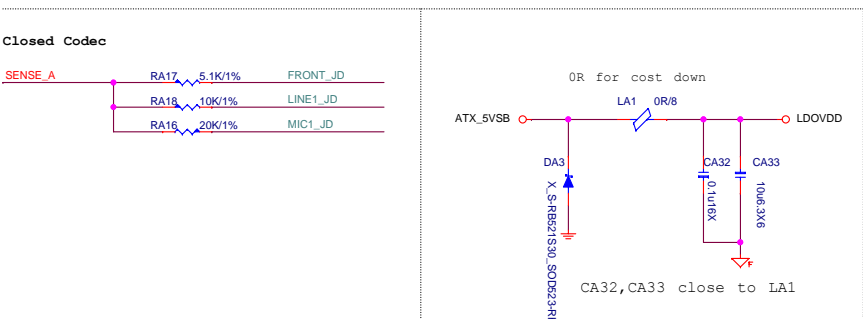
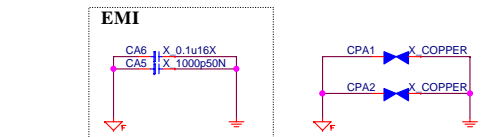
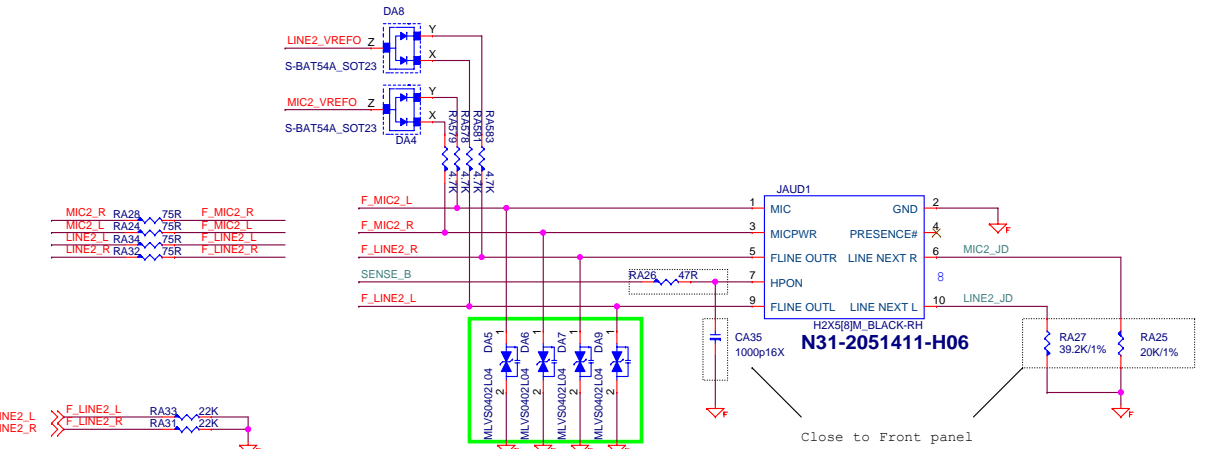
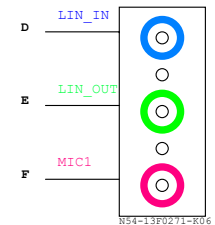
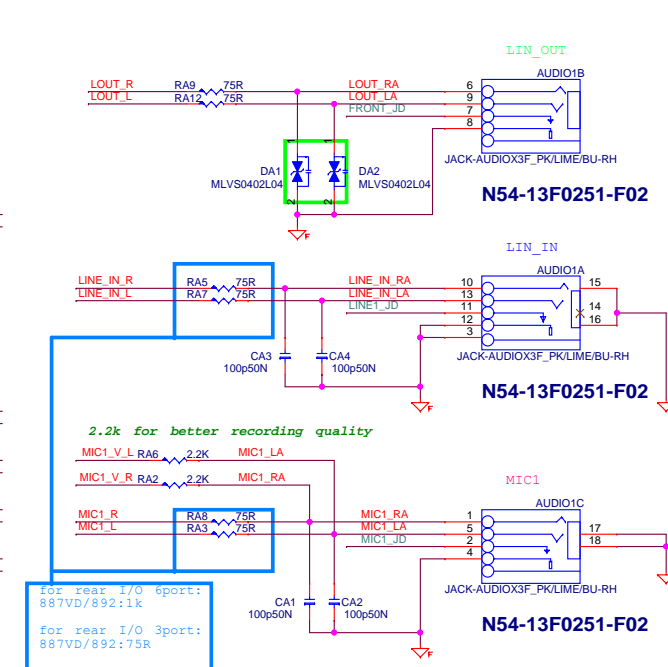
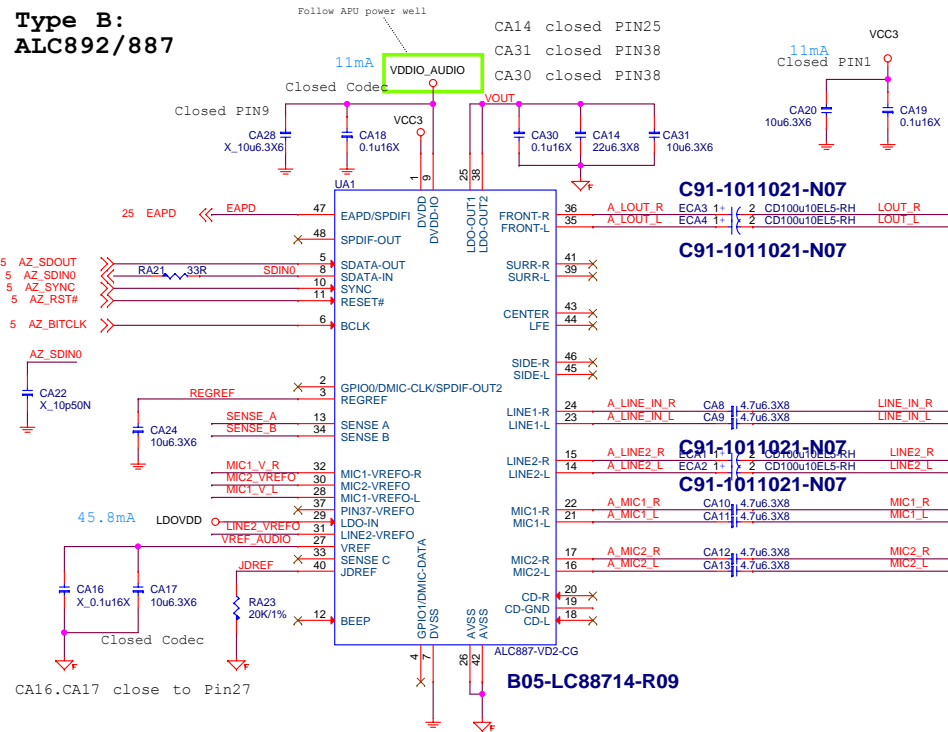
Title: LAN-RTL8111H

Size: Custom  
Document Number: MS-7B07  
Date: Thursday, April 27, 2017

Rev: 1.0  
Sheet: 23 of 52



Type B:  
ALC892/887

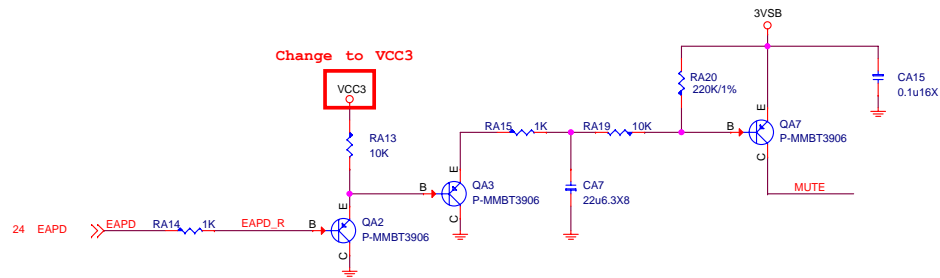


Varister --> cap for cost down  
**D0G-2710510-I05**  
**D0G-2950500-SI0**  
 Close to Jack



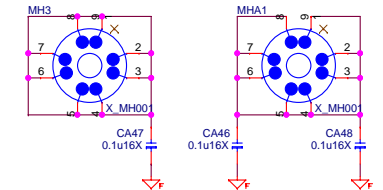
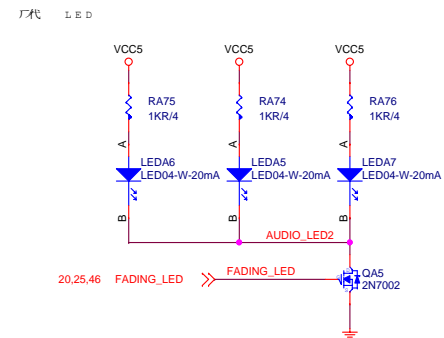
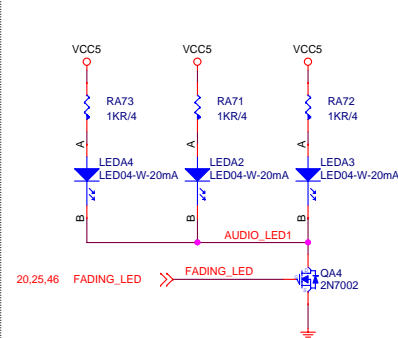
### Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



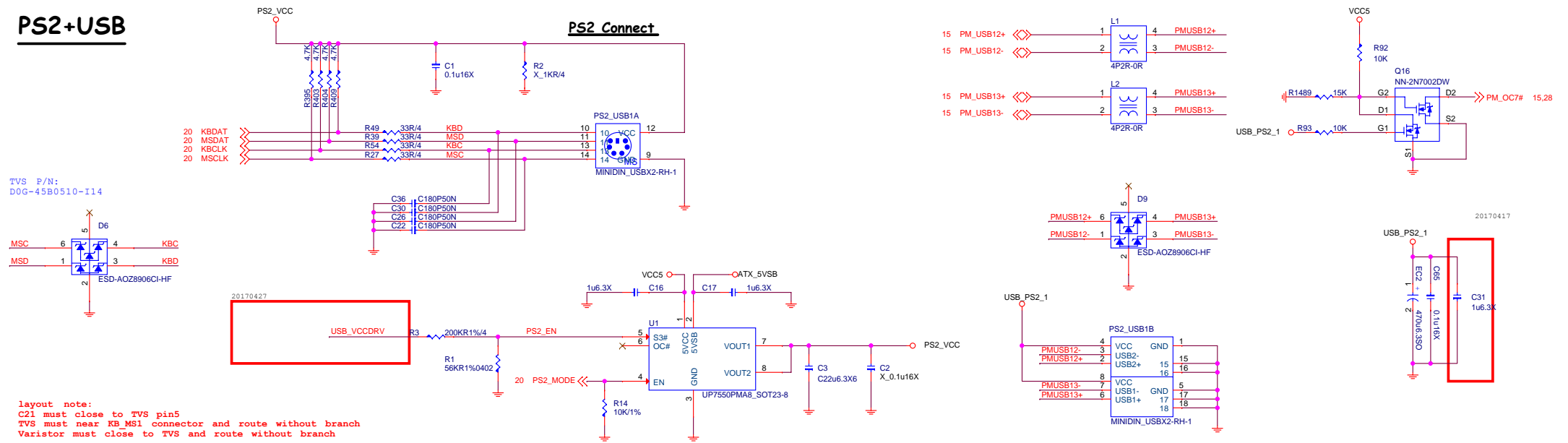
Digital

Analog

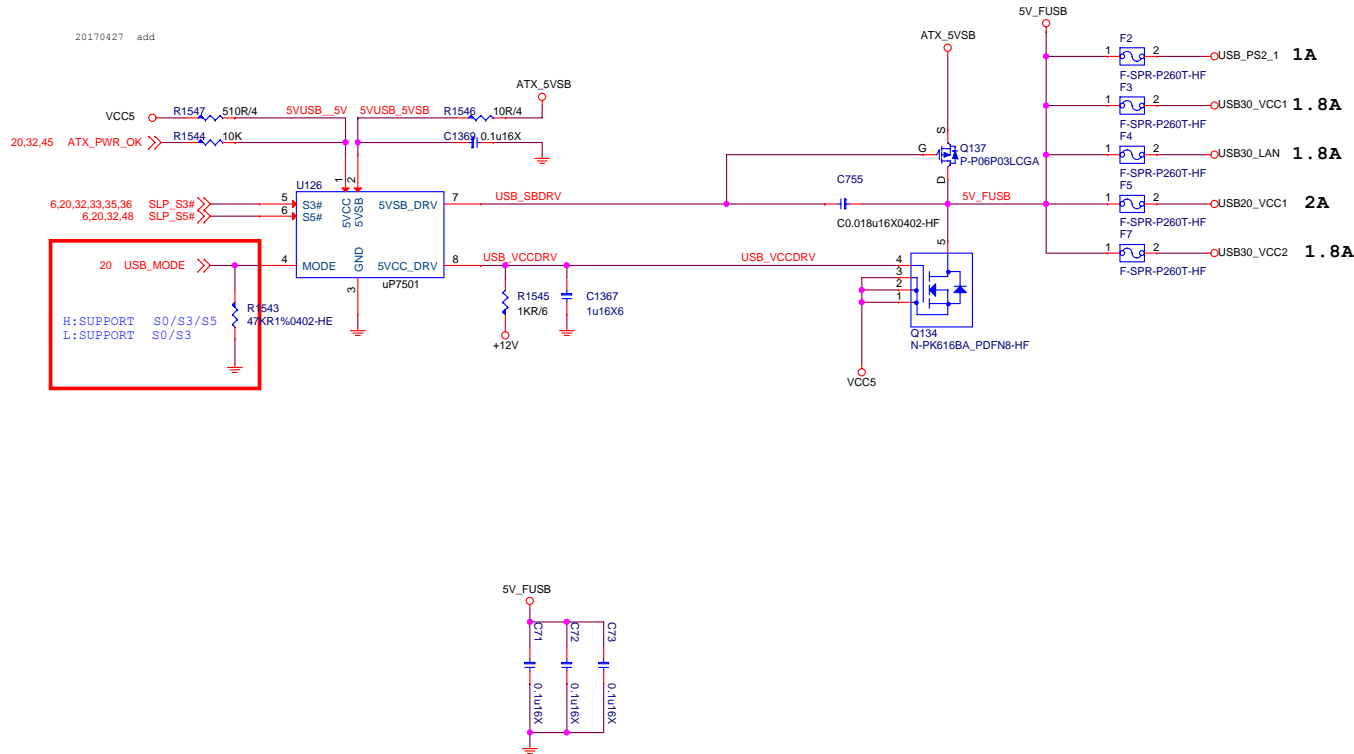




## PS2+USB

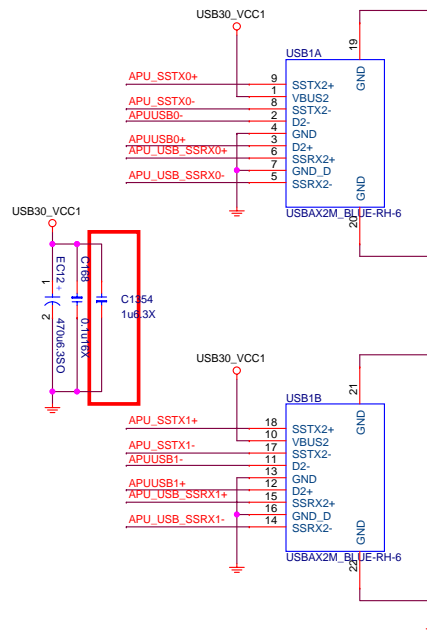
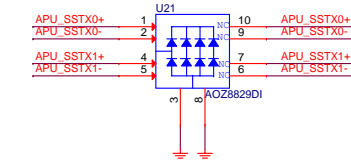
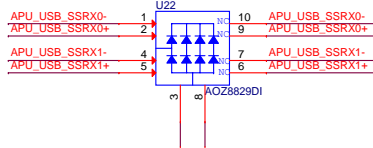
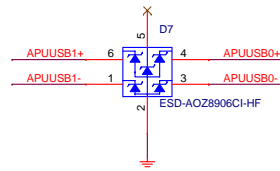
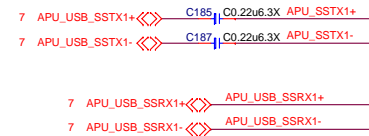
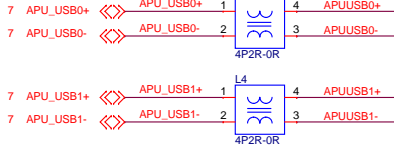
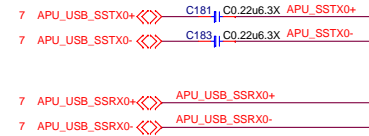


## USB Power

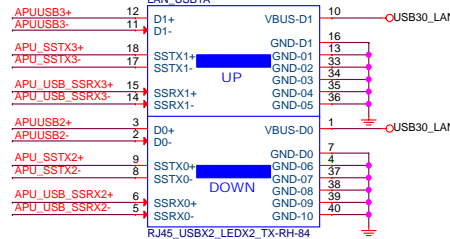
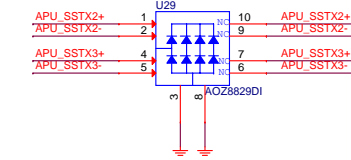
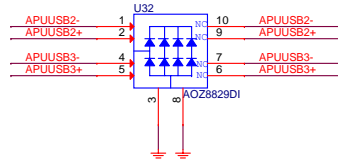
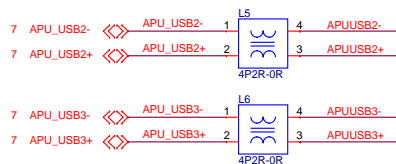
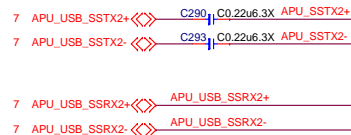




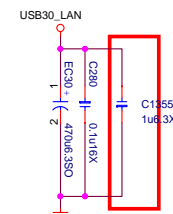
## USB 3.0



## USB3.1 GEN1

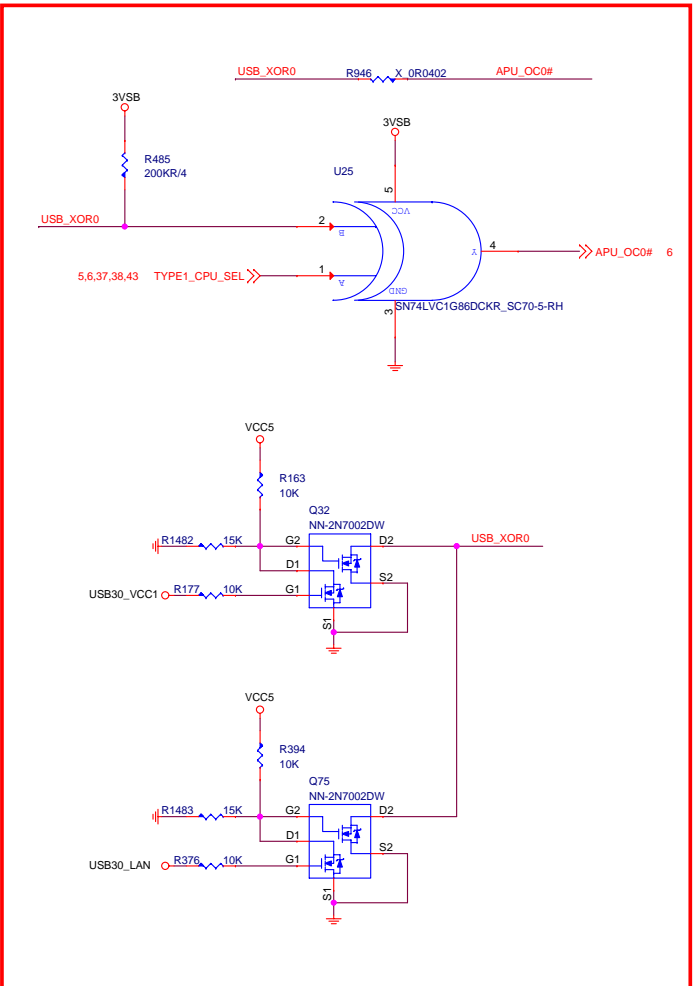


## LAN+USB



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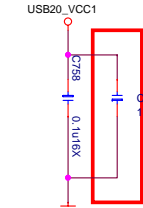
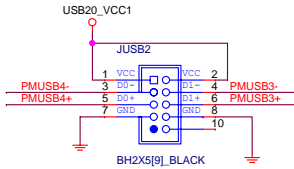
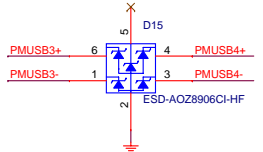
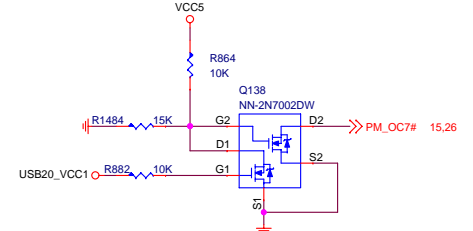
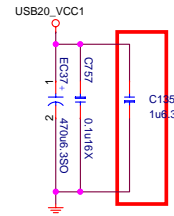
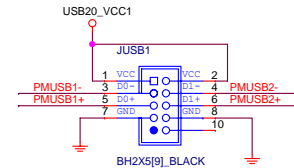
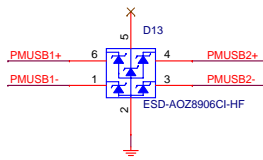
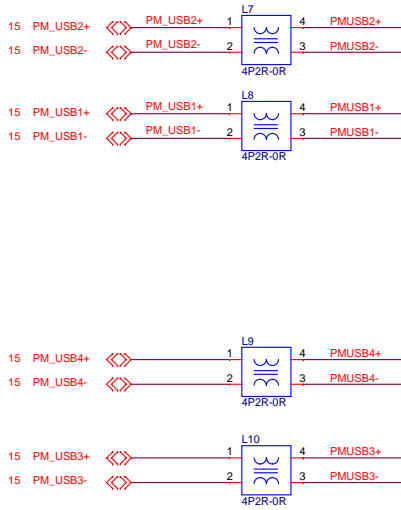
Modify USB\_OC# circuit



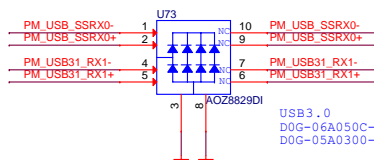
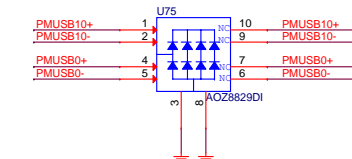
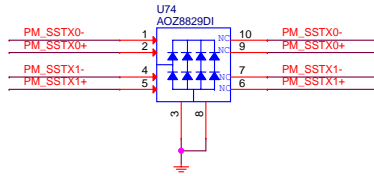
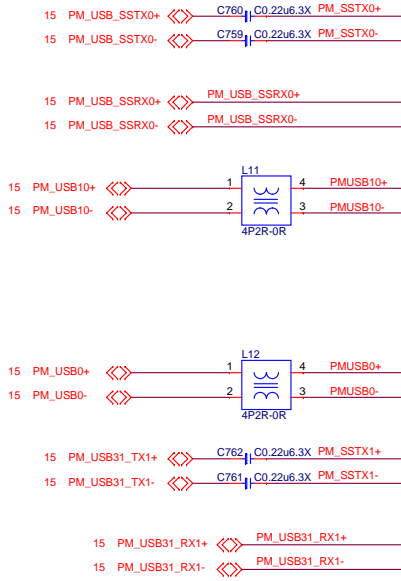
	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0



Front USB2.0

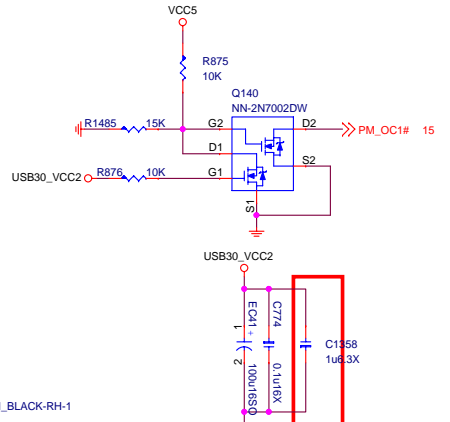
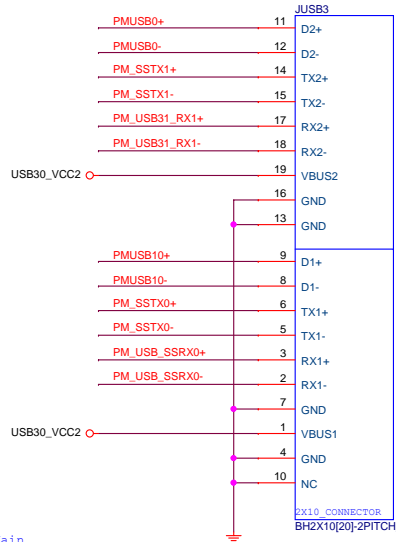


Front USB3.1 GEN1



USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL

USB2.0  
D0G-0200529-A68 Main  
D0G-0100619-I05 AVL



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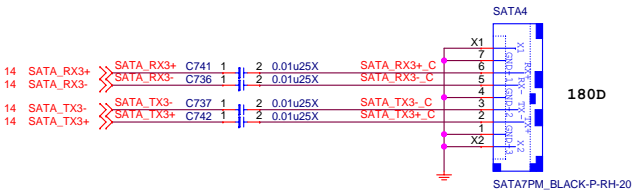
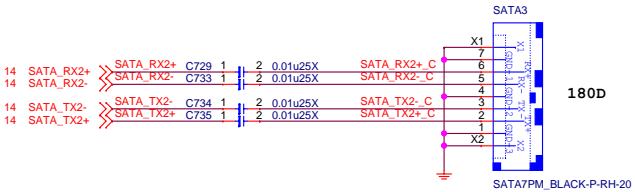
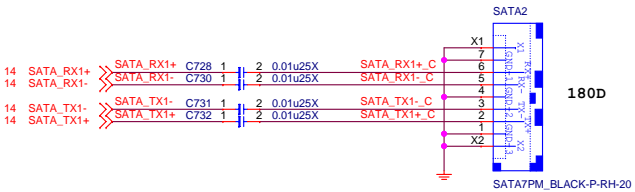
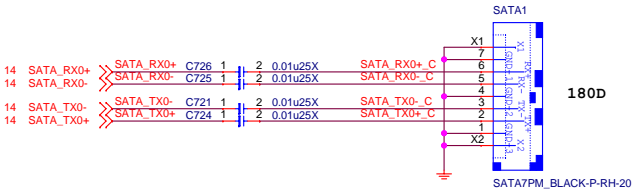
Title  
USB Front Side

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SATA Connector

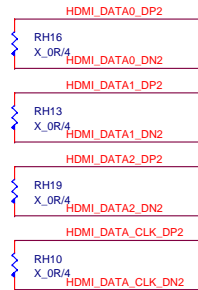
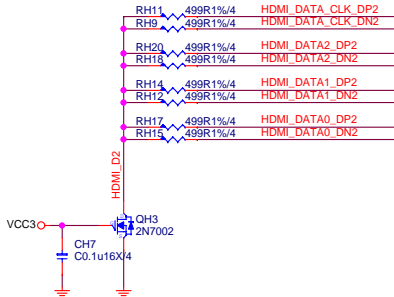
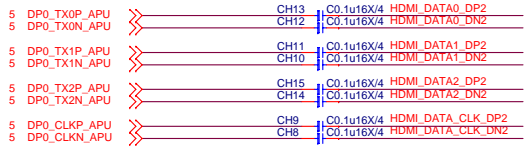


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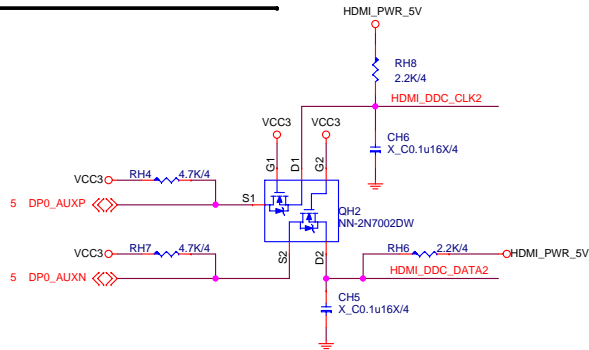


# HDMI CONNECTOR

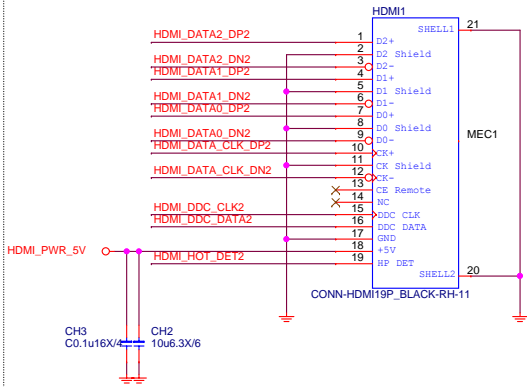
For HDMI 1.4



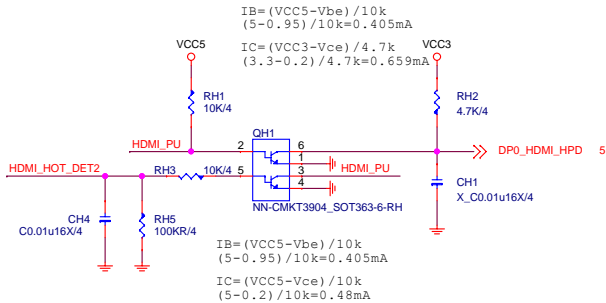
# AUX Level Shifter



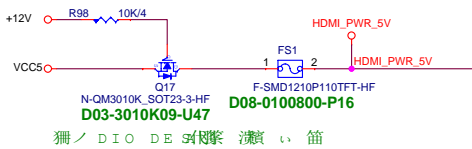
# Connector



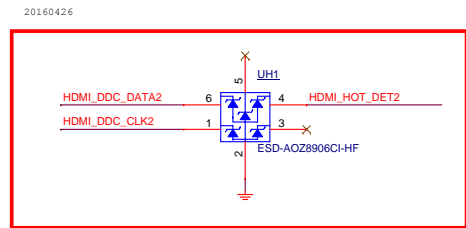
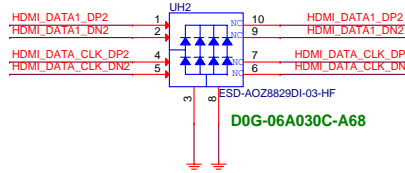
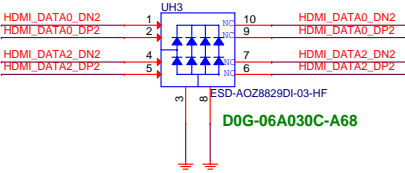
# HPD Circuit



# Connector Power



# For EMI

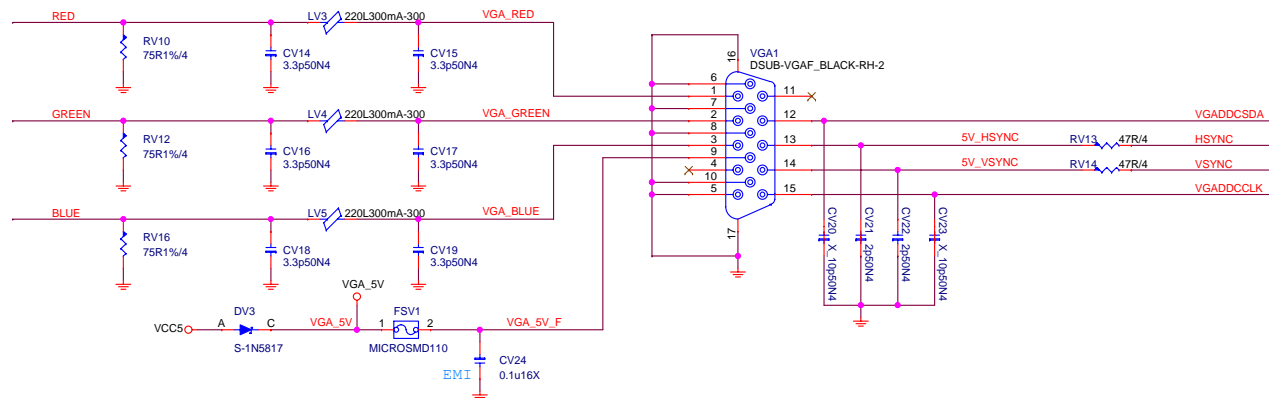




If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

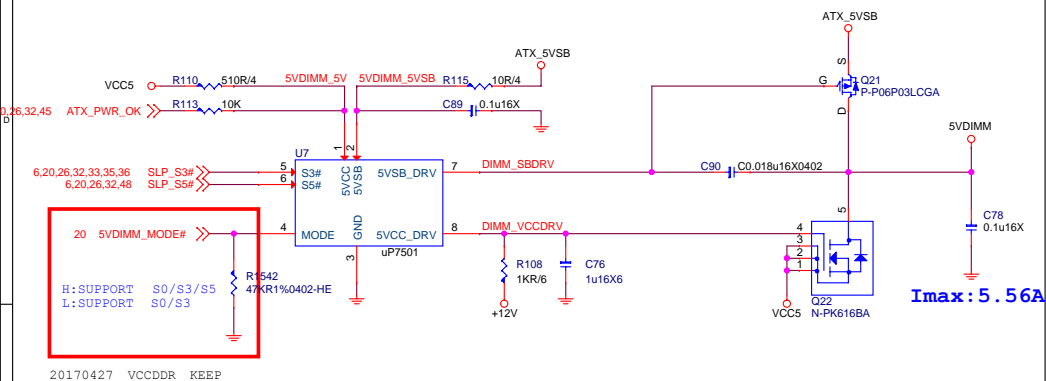


20160426

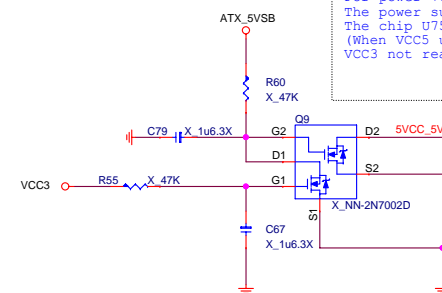
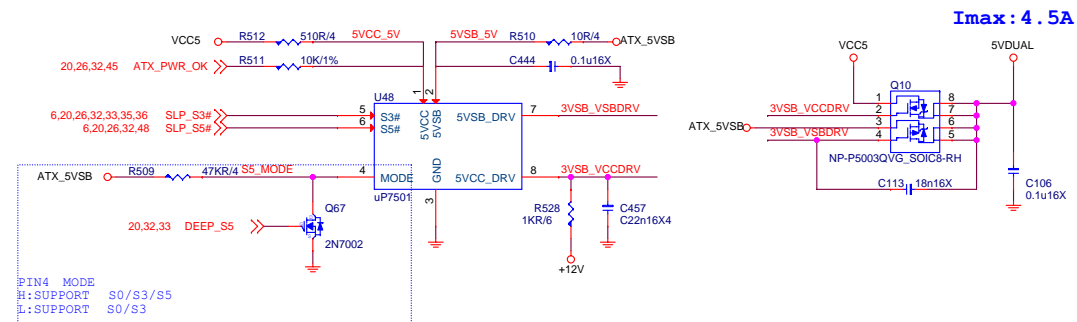




## 5VDIMM FOR DDR

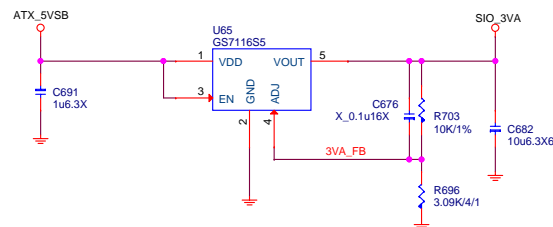


5VDUAL For 3VSB CPU 1.8V VDDP

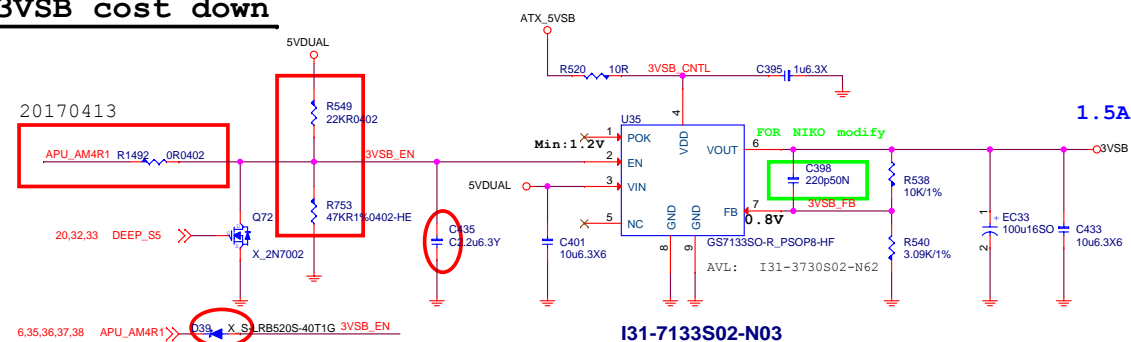


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.

SIO\_3VA



3VSB cost down

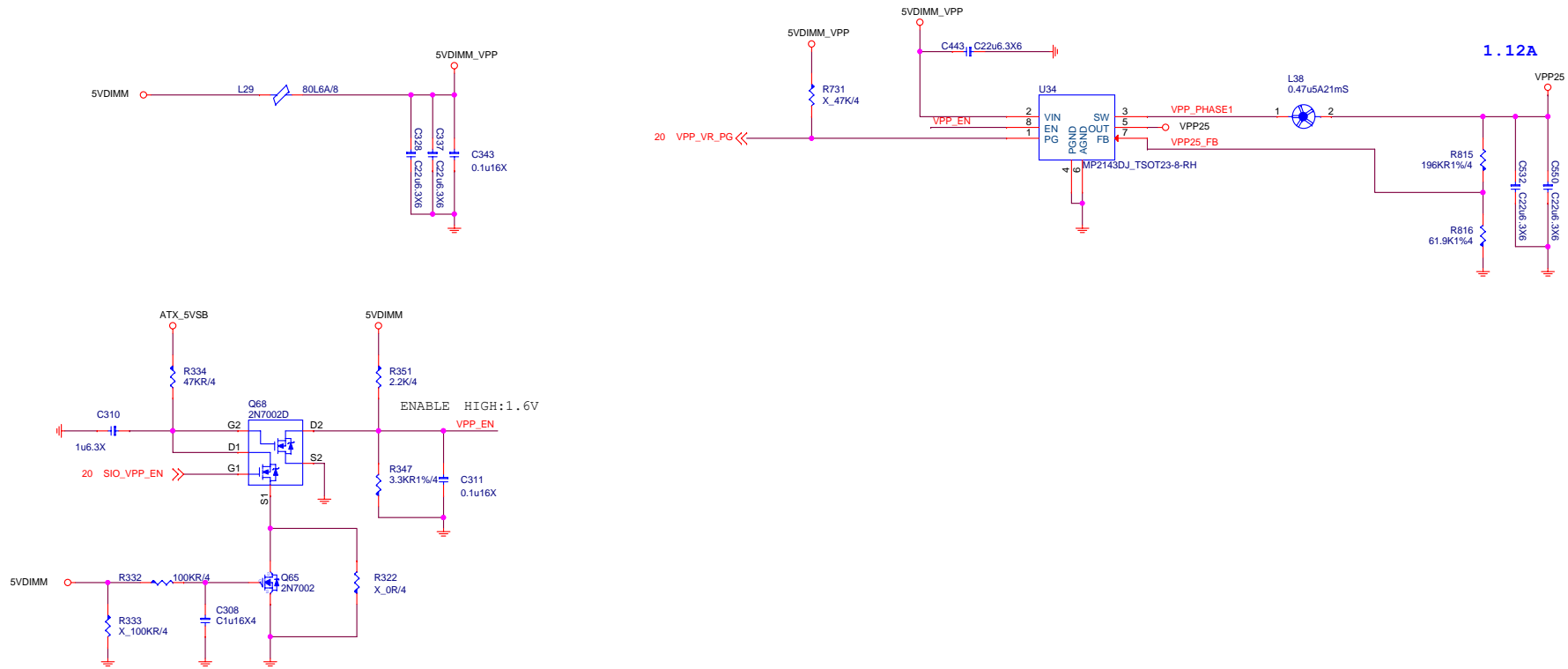








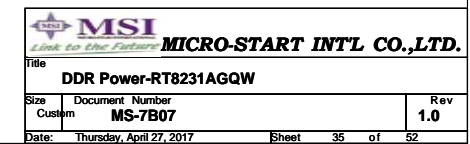
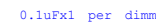
2DIMM :1.12A FOR DDR VPP2.5V





**0.6A FOR DDR VTT**

OCP:27.5A  
*I<sub>max</sub>: 20.85A*

2v



FOR CPU 1.8V S5

0.5A

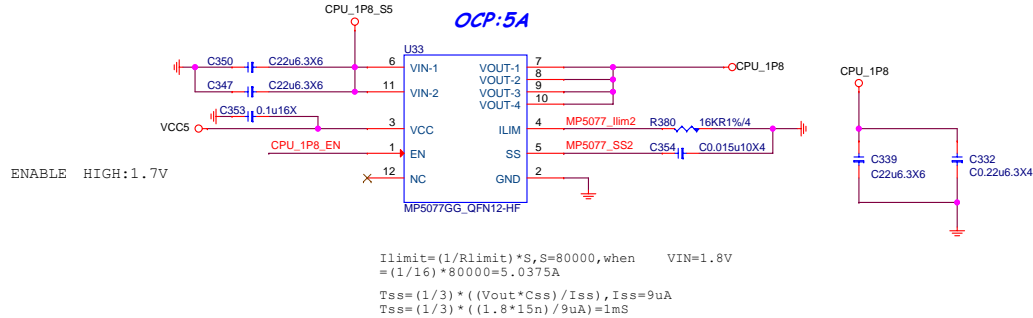
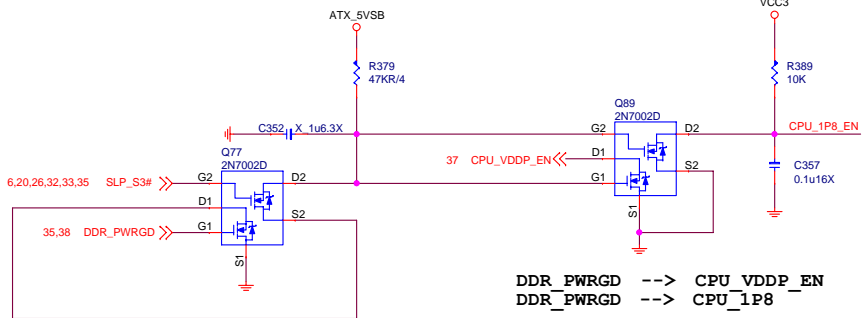
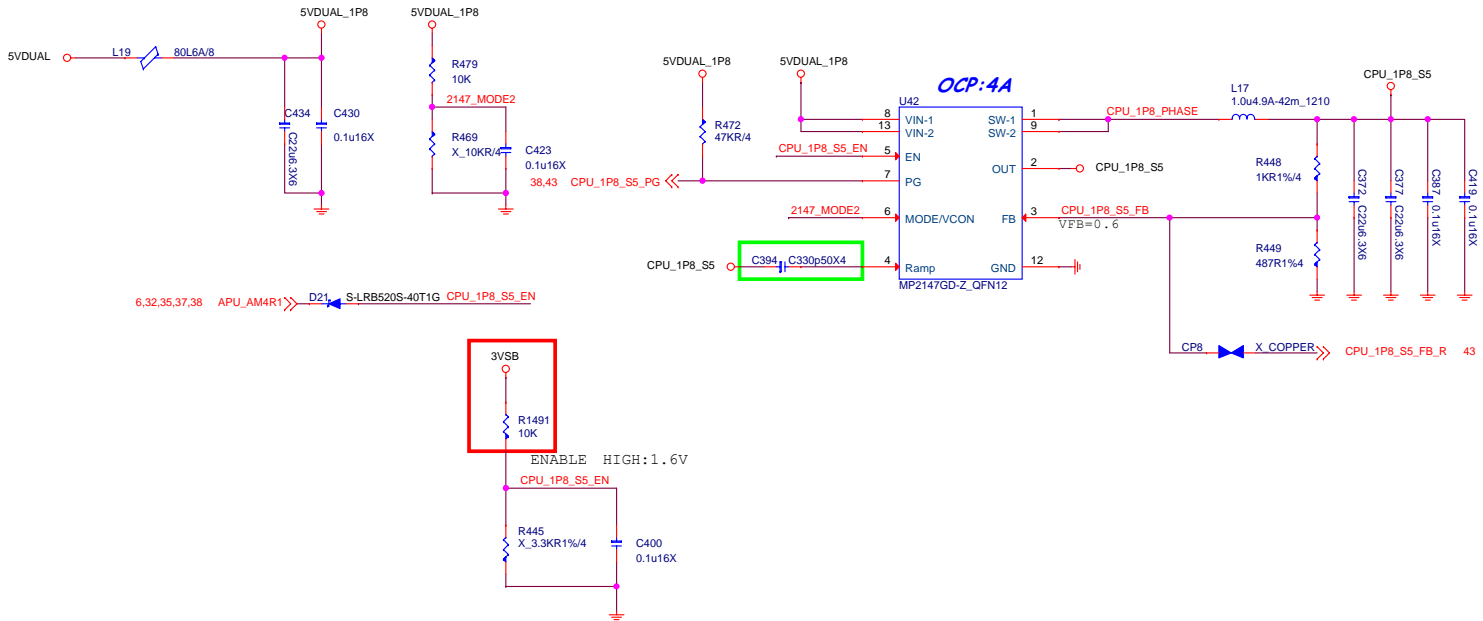
FOR VCCP\_SOC\_S5

0.9A

FOR CPU 1.8V S0

2.0A

0.5A + 2.0A + 0.9A = 3.4A



Ilimit=(1/Rlimit)\*S,S=80000,when VIN=1.8V  
=(1/16)\*80000=5.0375A  
Tss=(1/3)\*((Vout\*Css)/Iss),Iss=9uA  
Tss=(1/3)\*((1.8\*15n)/9uA)=1ms

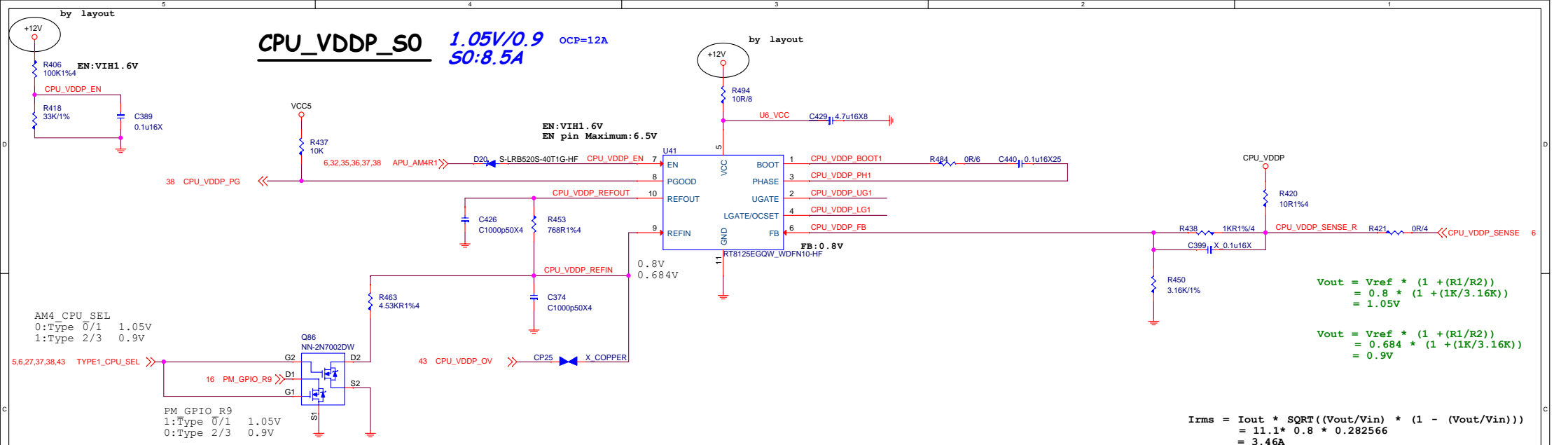
DDR\_PWRGD --> CPU\_VDDP\_EN  
DDR\_PWRGD --> CPU\_1P8



# CPU\_VDDP\_S0

1.05V/0.9  
S0:8.5A

OCP=12A



$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.8 * (1 + (1K/3.16K))$$

$$= 1.05V$$

$$V_{out} = V_{ref} * (1 + (R1/R2))$$

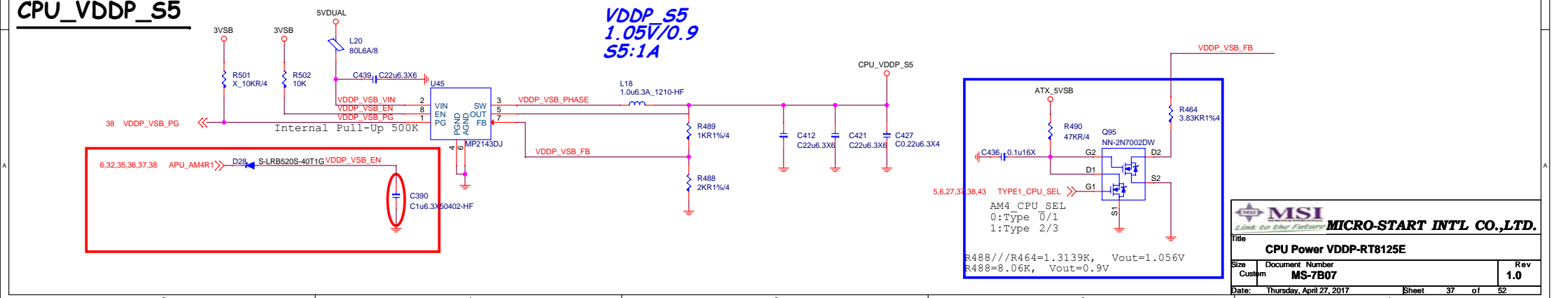
$$= 0.684 * (1 + (1K/3.16K))$$

$$= 0.9V$$

OCP=12A  
1.05V, 8.5A

# CPU\_VDDP\_S5

VDDP\_S5  
1.05V/0.9  
S5:1A



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Title: **CPU Power VDDP-RT8125E**

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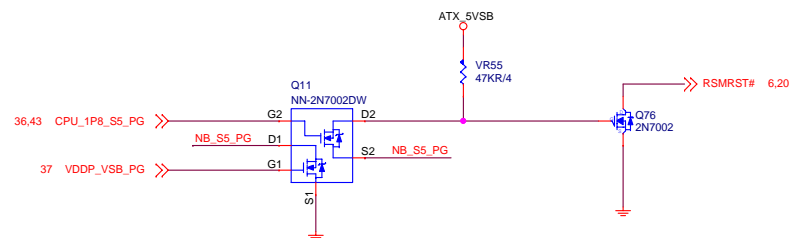
[illegible]

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

teknisi indonesia

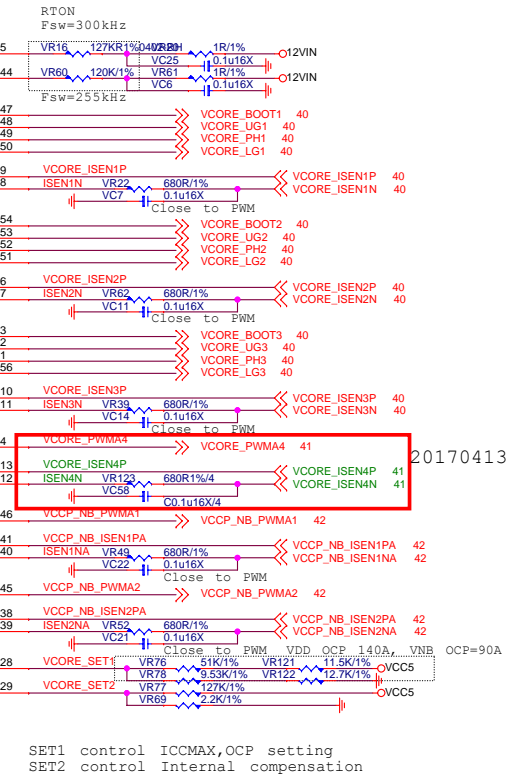
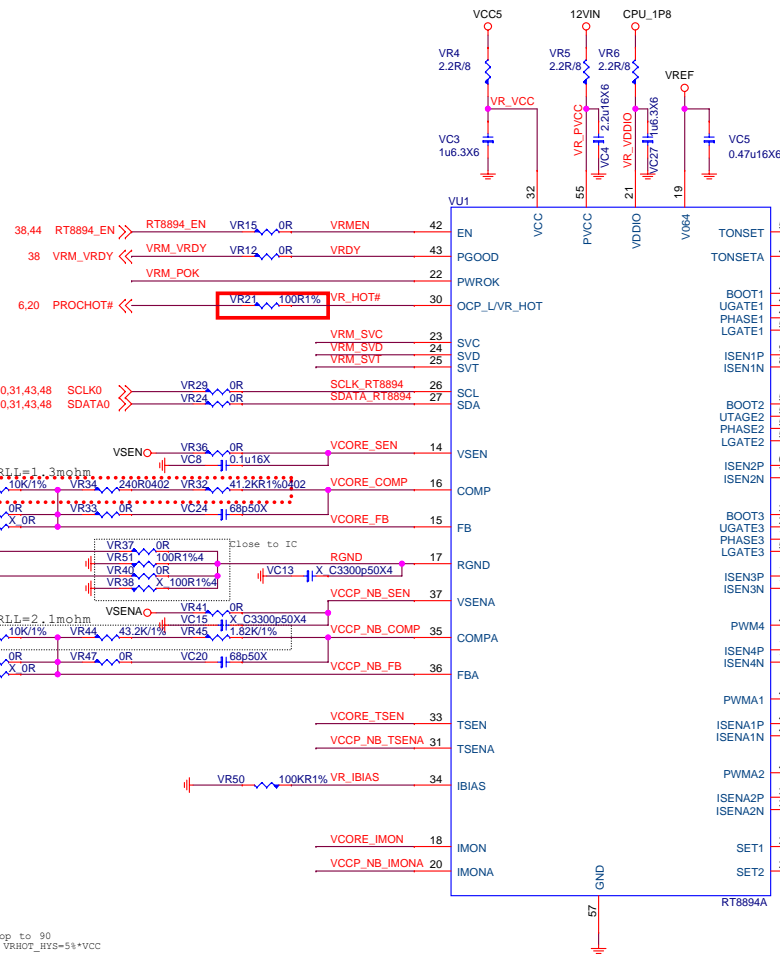
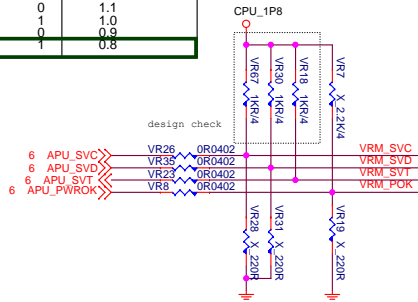
When you use external buffer  
then you cannot let APU PWR\_GOOD pin float  
in any sleep state.  
If you're buffer use 3.3V\_S0 and you need Pull-down 100K  
If you're buffer use 3.3V\_S5 and you don't need PD.

**S5 PG**

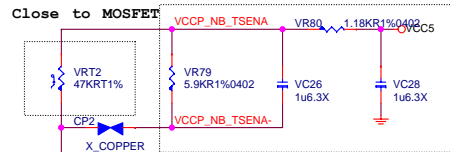
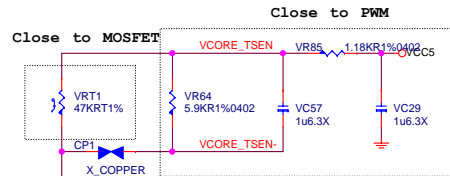




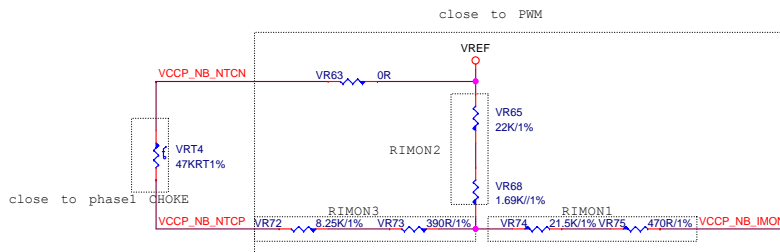
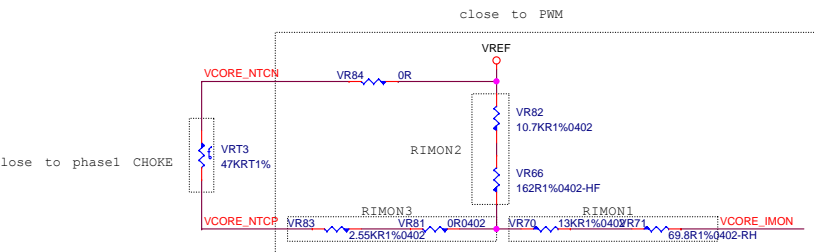
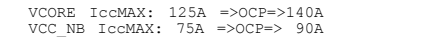
		BOOT VOLTAGE
SVC	SVD	Pre_PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



```
VR_HOT# pull low when T>110
VR_HOT# pull high when T drop to 90
Choose VRHOT_LOW=51%*VCC and VRHOT_HYS=5%*VCC
```

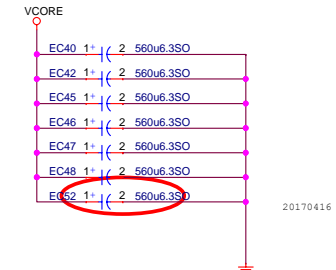
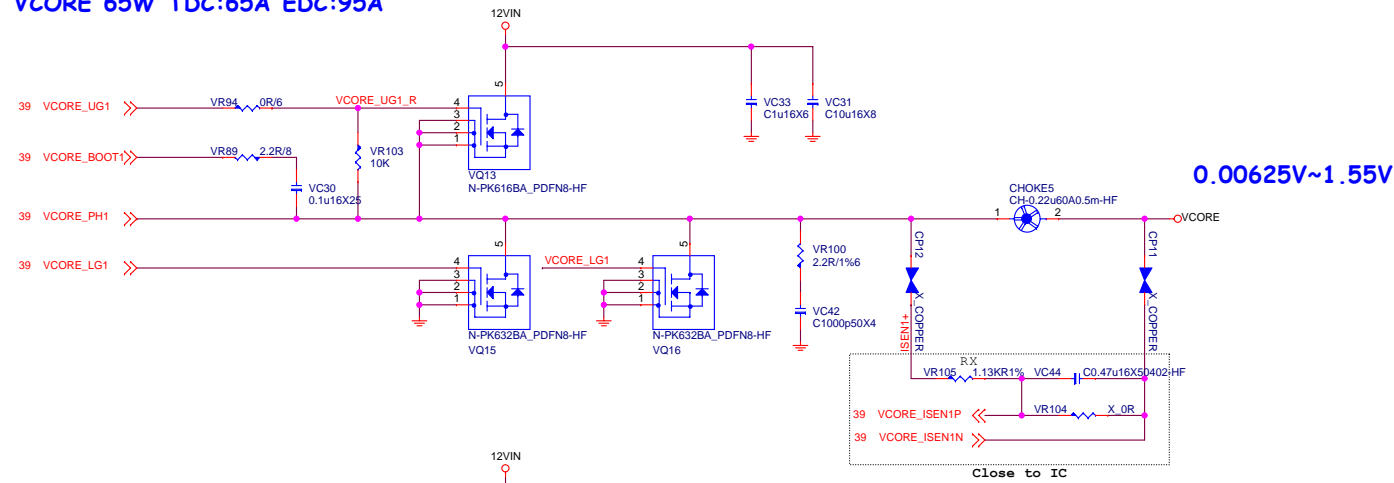


SMB Address: 0X40

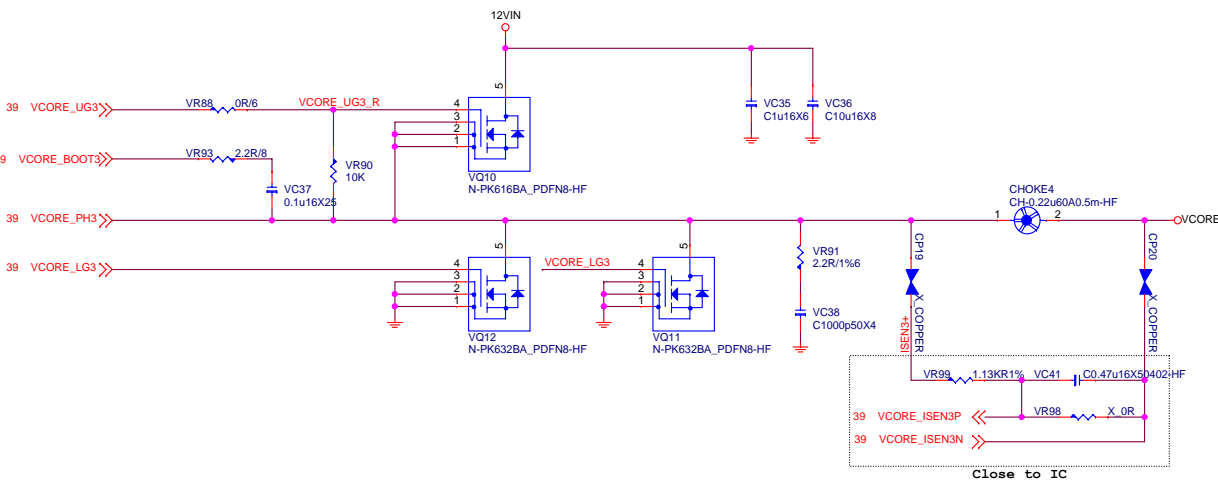




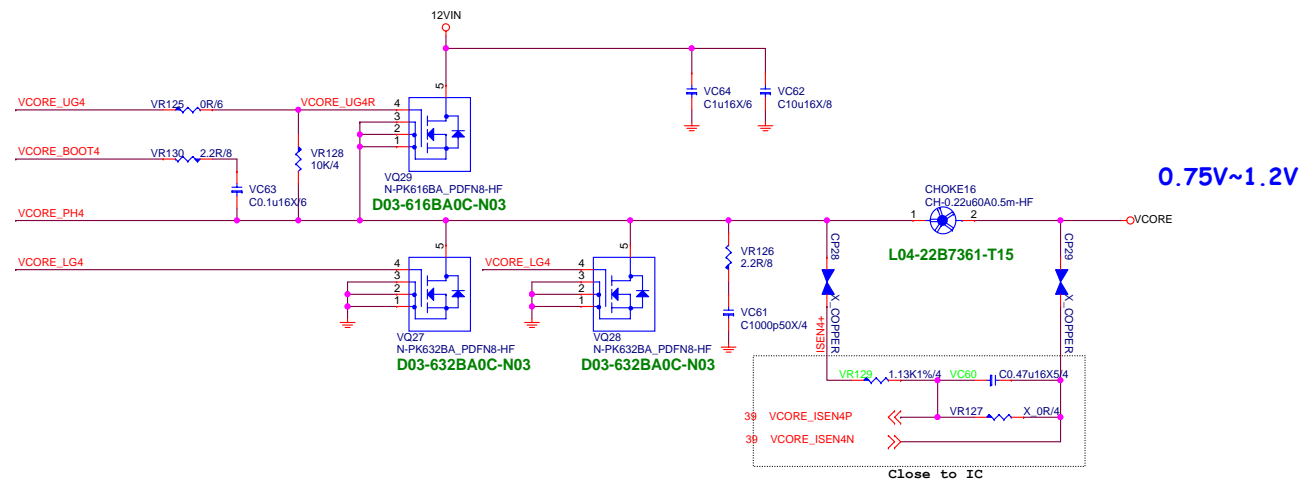
VCORE 95W TDC:80A EDC:125A  
VCORE 65W TDC:65A EDC:95A



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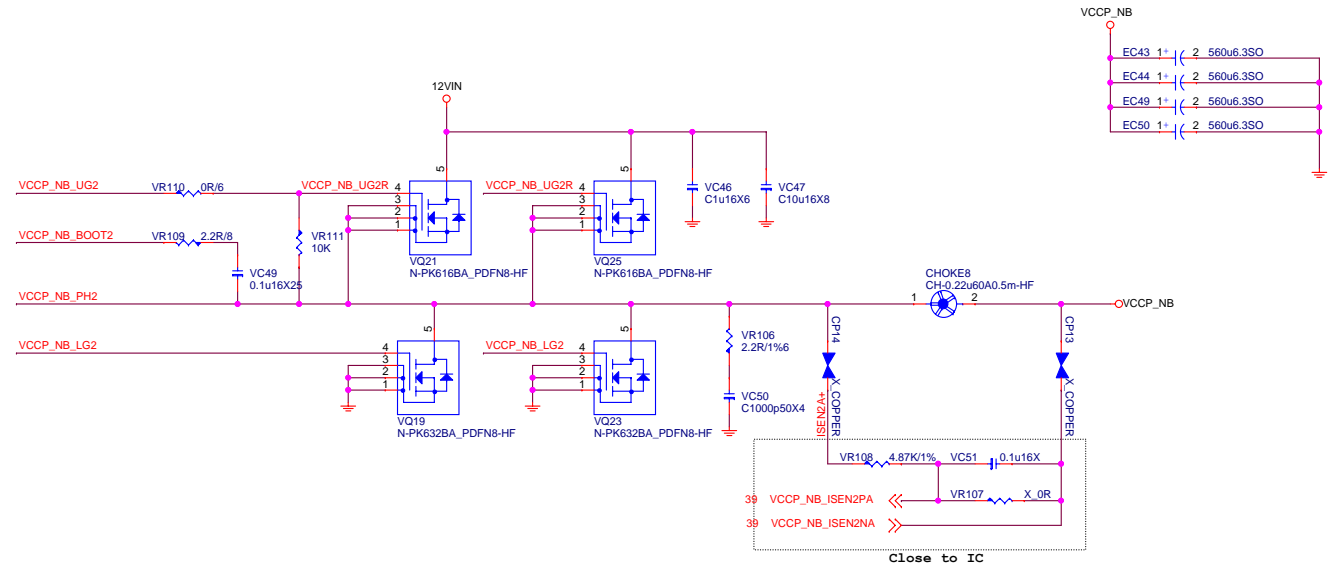
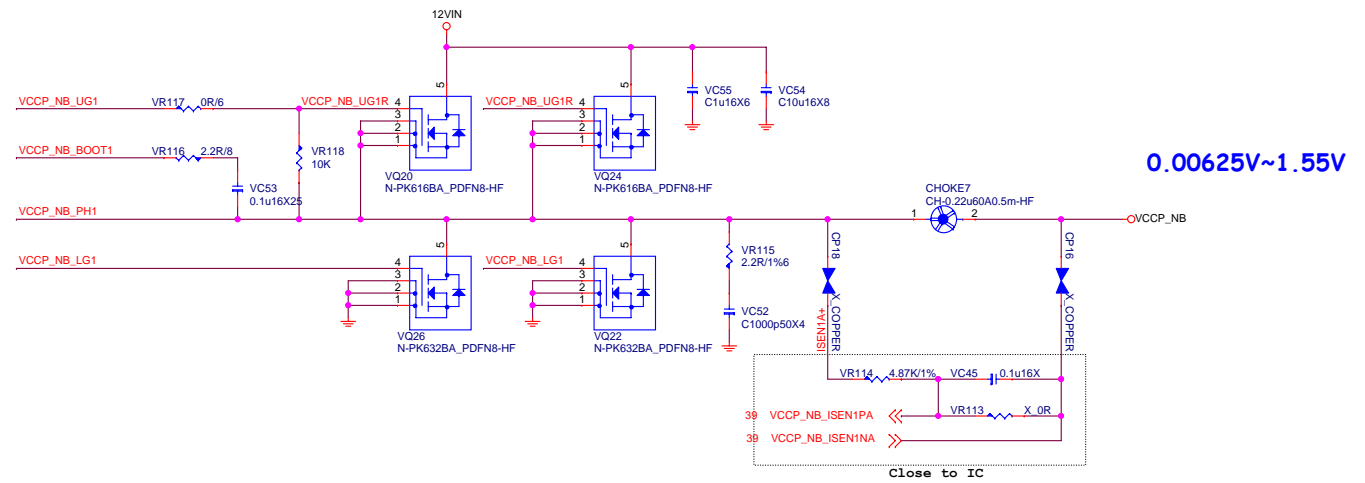
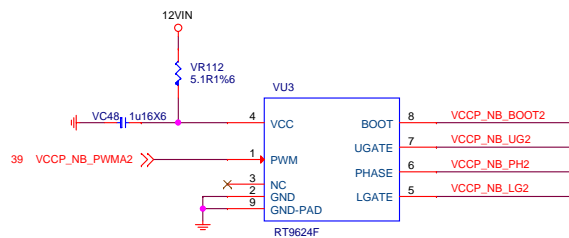
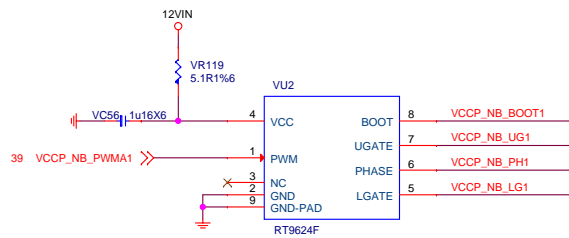








VCCP\_NB 95W TDC:50A EDC:75A  
VCCP\_NB 65W TDC:50A EDC:75A



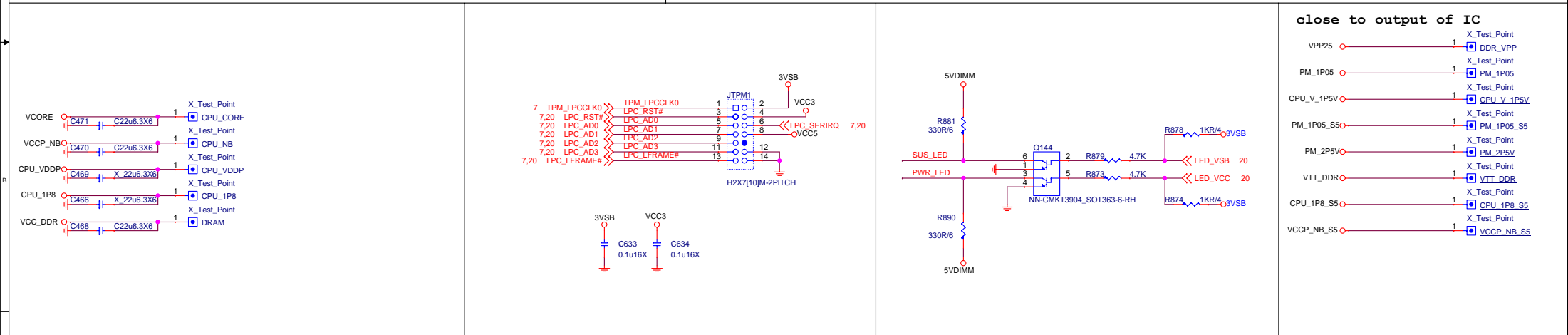
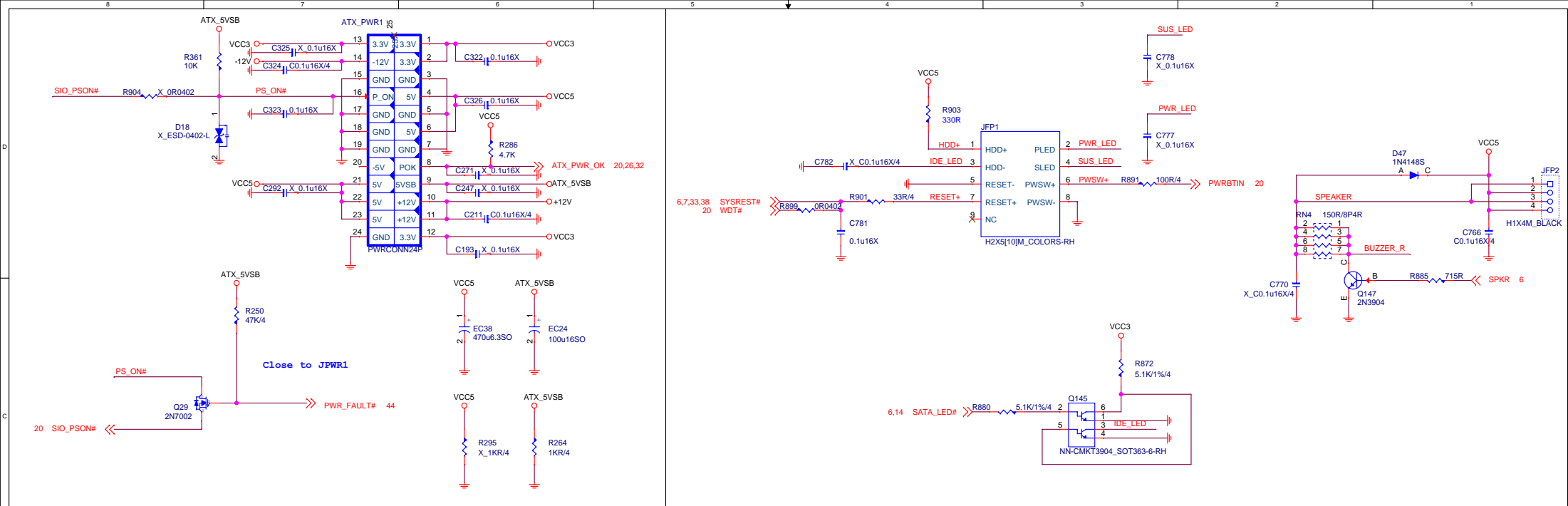


Title			
CPU Power NB Switch / NCT3933 OV			
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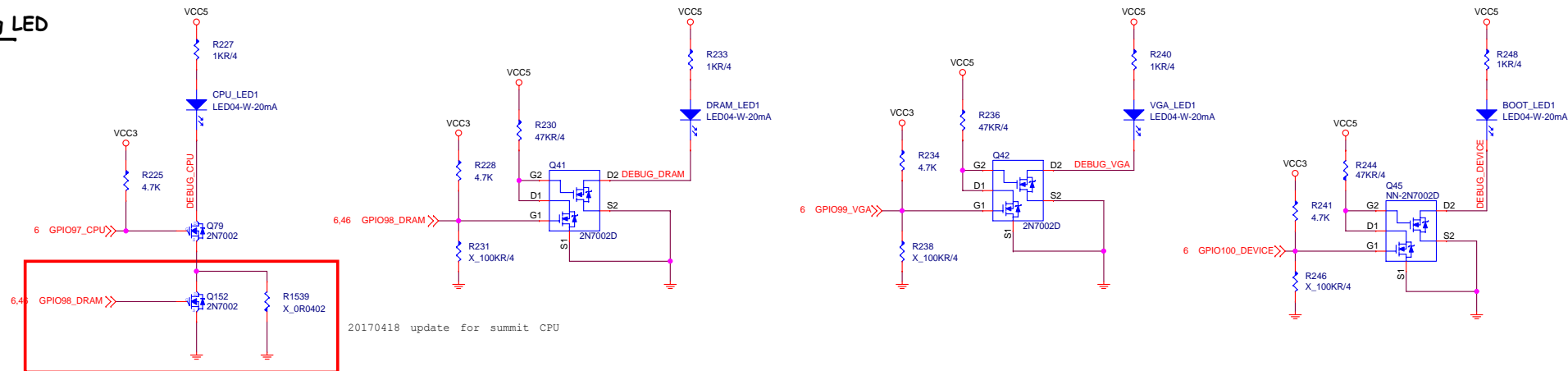








## EZ Debug LED

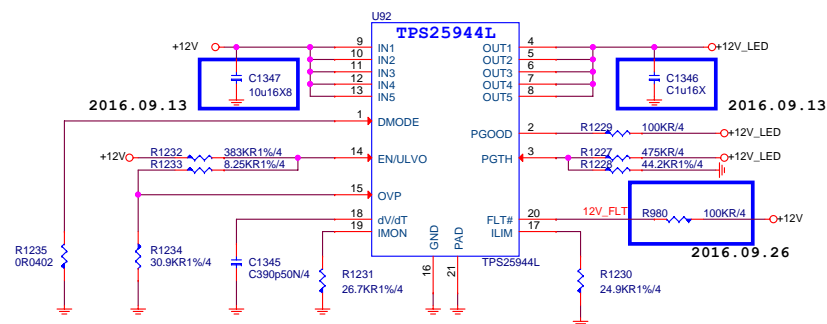


## LED Control by SIO

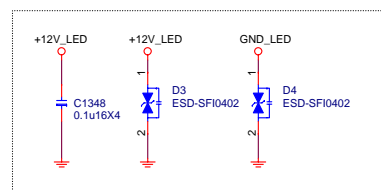
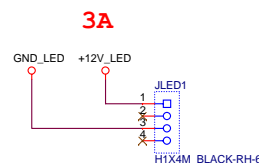
**JLED**

2016.07.06 Use TPS25944L

LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
獵	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
防威	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)



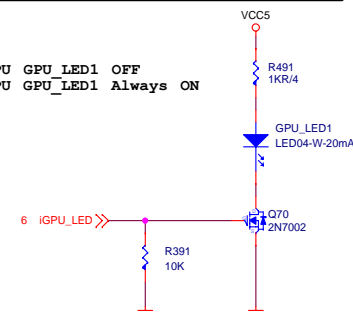
teknisi indonesia



```
.....
close to JLED1
```

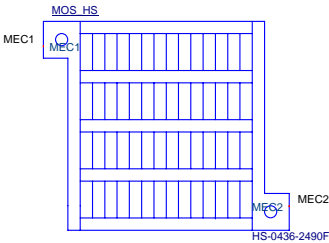
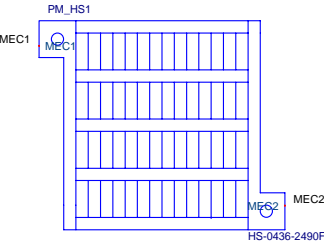
## AM4 APU Detect LED Circuit

```
iGPU GPU_LED1 OFF
dGPU GPU_LED1 Always ON
```

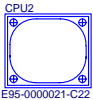




HEAT SINK

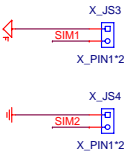


CPU Socket



RETENTION MODULE

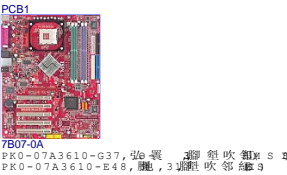
Simulation



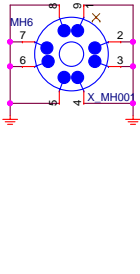
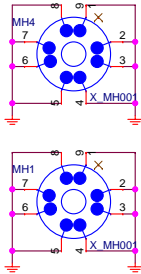
MANUAL PART



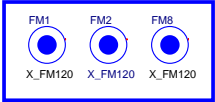
MOS HS(VCORE)



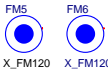
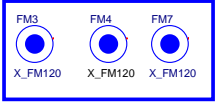
Optics Orientation Holes




5010



5020



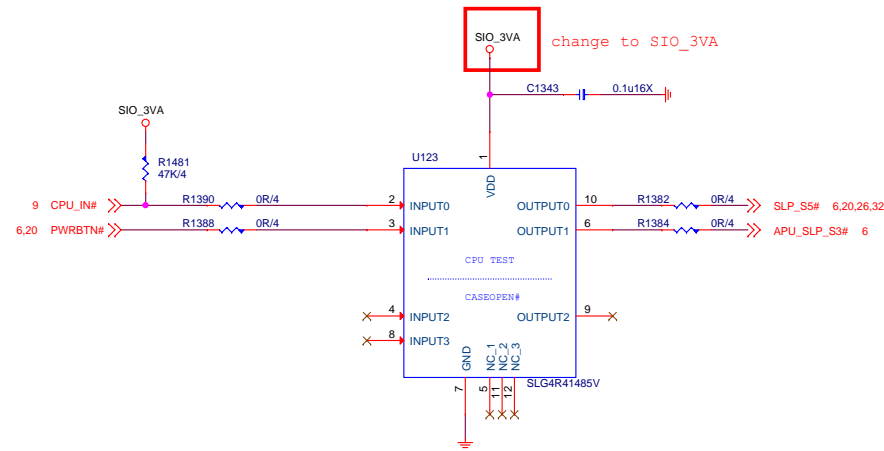
OPT	Configure	BOM	Function
		601-7A36-A01	XXXX
		601-7A36-01S	MS-7A36 1.0 A320 A320M PRO-VD,A320,AM4,2DDR4,1PCI-Ex16,2PCI-Ex1,4SATA3,6USB3.1 Gen1,HD Audio,GB LAN,DVI-D,VGA
		601-7A36-010	MS-7A36 1.0 A320 A320M PRO-VD,A320,AM4,2DDR4,1PCI-Ex16,2PCI-Ex1,4SATA3,6USB3.1 Gen1,HD Audio,GB LAN,DVI-D,VGA



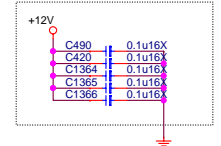
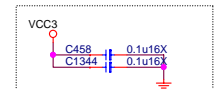
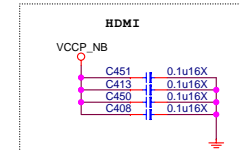
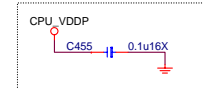
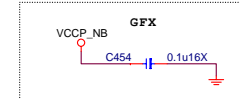
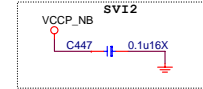
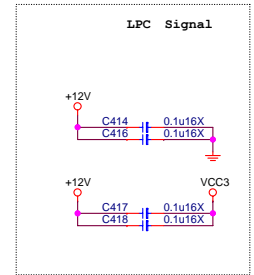
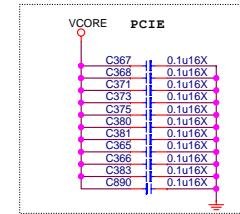
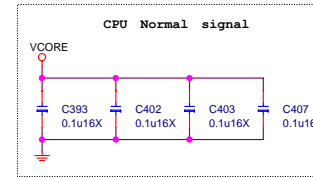
**MICRO-START INTL CO.,LTD.**

Title			BOM OPTION		
Size	Document	Number	Rev		
Custom	MS-7B07		1.0		
Date:	Thursday, April 27, 2017		Sheet	47	of 52





## Moat Cap



## RTC & Clear CMOS Circuit

20170413 PIN7floating PIN3 resever pull down

